Engineering of microfabricated ion traps and integration of advanced on-chip features

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Abstract | Atomic ions trapped in electromagnetic potentials have long been used for fundamental studies in quantum physics. Over the past two decades, trapped ions have been successfully used to implement technologies such as quantum computing, quantum simulation, atomic clocks, mass spectrometers and quantum sensors. Advanced fabrication techniques, taken from other established or emerging disciplines, are used to create new, reliable ion-trap devices aimed at large-scale integration and compatibility with commercial fabrication. This Technical Review covers the fundamentals of ion trapping before discussing the design of ion traps for the aforementioned applications. We overview the current microfabrication techniques and the various considerations behind the choice of materials and processes. Finally, we discuss current efforts to include advanced, on-chip features in next-generation ion traps.

The trapping of atomic ions in confining electric fields in vacuum was first conceived and demonstrated by Wolfgang Paul and Hans Georg Dehmelt, earning them a share of the 1989 Nobel prize in physics[1,2]. An ion isolated in this way can be extremely well decoupled from its environment and thus cooled to very low temperatures through laser techniques (such as those in REF.[3]). The extreme isolation and low thermal energy mean that the energy levels of the laser-cooled ion are highly stable and well resolved, with quantum states that have been observed to remain coherent over several minutes[4,5]. These properties, along with the ability to prepare and detect the quantum states and generate high-fidelity entanglement between trapped ions, make trapped-ion systems particularly well-suited for experiments that require the precise control of well-defined quantum systems, such as atomic clocks[6], quantum sensors[7], quantum simulators[8–11], mass spectrometers[12–14] and quantum computers[15,16].

The traditional ion-trap design introduced by Paul, the Paul trap, uses oscillating (RF) voltages to create potential minima in up to three dimensions (FIG. 1), which, when combined with static d.c. fields, are able to confine the ion to a certain position in space[1]. With numerous applications of trapped ions comes the desire to greatly increase the number of ions while maintaining (and in some cases increasing) the precise control over the position of individual ions. Quantum computing is a good example in which many approaches to scalability require such a level of control[17–19]. The precise control of the ion positions requires a considerable reduction in the size and an increase in the number of control electrodes, making the early type of Paul traps, consisting of mechanically machined 3D electrode structures, unsuitable[20]. Instead, microfabrication methods allow the realization of the feature sizes, reproducibility and mass producibility needed for such devices. This led to an early prototype, in 1999, which was made with laser-machined, gold-on-alumina wafers[21]. It was followed in 2006 by monolithic ion microchips that were lithographically patterned[22,23]. While quantum computing provided the initial motivation for using microfabricated devices in ion traps, other trapped-ion technologies took advantage of these developments. For instance, lithographic methods contributed to the realization of a compact ion-trap package for portable atomic clocks[24,25], and also quantum simulations in 2D lattices with micrometre-scale separation between ions[26,27].

These ‘trap-on-chip’ devices use established fabrication techniques from the semiconductor and micro-electro-mechanical system (MEMS) industries to realize micrometre-scale architectures in both 2D (surface traps)[23,28] and 3D configurations[22,29]. Another set of well-established techniques, also highly prevalent in modern electronics, comes from complementary metal–oxide–semiconductor (CMOS) technology and has been used to successfully fabricate an ion trap[30]. These methods have allowed the creation of reliable ion traps using established processes, giving trapped ions a prominent position in quantum technologies.

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https://doi.org/10.1038/s42254-020-0182-8

Key points

- Trapped atomic ions are a highly versatile tool for a wide variety of fields from fundamental physics to quantum technologies.
- Ion traps use electric and magnetic fields to provide 3D confinement of ions in free space. Ion traps can be fabricated with greater ease by using a surface electrode structure integrated within a microchip.
- The realization of several quantum technologies that use trapped ions requires the integration of advanced features such as optics and electronics into such a microchip, either within a monolithic structure or through multi-wafer stacking.
- Development is in progress concerning the integration of multiple features, especially in terms of the compatibility of fabrication processes, chip modularity, functionality and exact specifications of the desired features.

In addition to the miniaturization of ion traps, the integration of peripheral components, such as photodetectors[31] and digital-to-analogue converters (DACs)[32] into the ion trap is also of great interest because it allows the creation of compact devices and stand-alone trap modules, and has the potential to reduce electrical noise[33]. The integration of peripheral components is also critical to large-scale quantum computing with trapped ions where stand-alone modules are a key ingredient of scalability[18,19].

To create a quantum computer with enough qubits to perform interesting operations, the ability to connect different individual modules is required. Two methods that address this connectivity have been proposed. One scheme[18,34] uses photons emitted by ions in separate modules to create inter-module entanglement. Another method[19] relies on shaping electrodes in such a way that when neighbouring modules are closely aligned, ions can be transported from one module to another by electric fields.

This Technical Review overviews the state-of-the-art of microfabricated ion traps, including efforts to integrate advanced features such as optical components and electrical devices. For further discussion of ion-trap supporting hardware, and other ion-trap fabrication methods, we suggest REFS[35–40].

Ion-trap geometries

In this section, we discuss basic ion-trap geometries for top-layer electrode design, and the geometrical considerations for ion transport and advanced ion-trap designs. The basics of ion trapping are covered in BOX 1, and a typical experimental setup is described in BOX 2. The evolution of ion-trap geometries is discussed in BOX 3.

Basic principles of five-wire geometry. Panel c of the figure in BOX 3 shows a simplified planar view of a surface ion trap in a symmetric, five-wire geometry. An RF voltage is applied to a pair of linear electrodes while all the other electrodes are held at RF ground. The ponderomotive potential generated by the RF voltage confines ions parallel to the z axis at a height given by the widths of the RF and central ground electrode. Assuming infinitely long rails, the zero potential line from the RF (that is, the RF nil) can be expanded along the longitudinal direction, and the axial position of the ions can be determined by static electric fields only. To generate the static electric field required for trapping or shuttling the ions in the axial direction, a calculated d.c. voltage set is applied to the segmented electrodes[41,42].

RF nil
Also known as RF null. The minimum energy of the RF pseudopotential, which gives the ion's position in an RF field.

Hessian matrix
Matrix of second-order partial derivatives, in this case derivatives of the total potential seen by the ion.

The five-wire electrode geometry of surface ion traps has been analytically modelled in numerous studies[28,43,44], including the modelling of electrostatics due to gaps between electrodes[45]. The widths of the RF and ground (denoted a and b, respectively, in panel **c** of the figure in BOX 3) electrodes in a gapless, five-wire geometry can be used to determine the trap depth, ψ_E, and ion height, h_{RFnil} (REF.[43]):

$$\psi_E = \frac{e^2V^2}{\pi^2 m\Omega^2}\frac{b^2}{(a+b)^2+(a+b)\sqrt{2ab+a^2}}, \quad (1)$$

$$h_{RFnil} = \frac{\sqrt{2ab+a^2}}{2}, \quad (2)$$

where the trap depth is the difference in the ponderomotive potential between the RF nil and the escape point (that is, where the energy of the ion is larger than the trapping potential), and Ω, e, m and V indicate the RF drive frequency in Hertz, elementary charge in Coulombs, ion mass in kilograms and RF voltage amplitude in volts, respectively.

A high trap depth is required to trap ions for a long time. For a low heating rate due to ion motion, a large ion–electrode distance is required. These parameters cannot be optimized simultaneously (especially given differing scaling laws), and compromises are determined by considering the constraints given by the specifics of the experimental setup[46,47]. It has been analytically demonstrated[47] that a ratio of RF and ground-rail widths of $b/a = 3.68$ provides a maximized trap depth. However, this wide ratio increases the distance between the outer d.c. electrodes and the trapped ions, thus reducing d.c. confinement. A solution to this replaces the central ground electrode with segmented d.c. electrodes, allowing for a minimized ion–electrode distance[42], but because of fabrication constraints, this is not always achievable. This balancing act is commonplace in ion-trap design and can depend heavily on the purpose of the experiment and voltage range available on the electrodes. The longitudinal (axial) direction is not usually considered during simple RF electrode design, since its properties are mainly determined by d.c. voltages.

Rotation of the principal axes. In a typical experimental setup with a surface ion trap, the allowed laser paths are limited to the direction parallel or perpendicular (through a vertical hole penetrating the substrate[42]) to the surface of the trap chip. To be able to effectively Doppler-cool an ion in all motional directions (principal axes), the laser path must interact with all the principal axes. This is achieved by rotating the principal axes of motion (FIG. 1). The rotation can be achieved by tilting the total electric potential at the ion position. The rotation angle can be calculated from the eigenvectors of the Hessian matrix of the total electric potential. To tilt the potential, there are two commonly used methods. The first approach uses RF rails of different widths, which rotates the potential[23,44,48]. The second method uses asymmetric d.c. voltages applied to

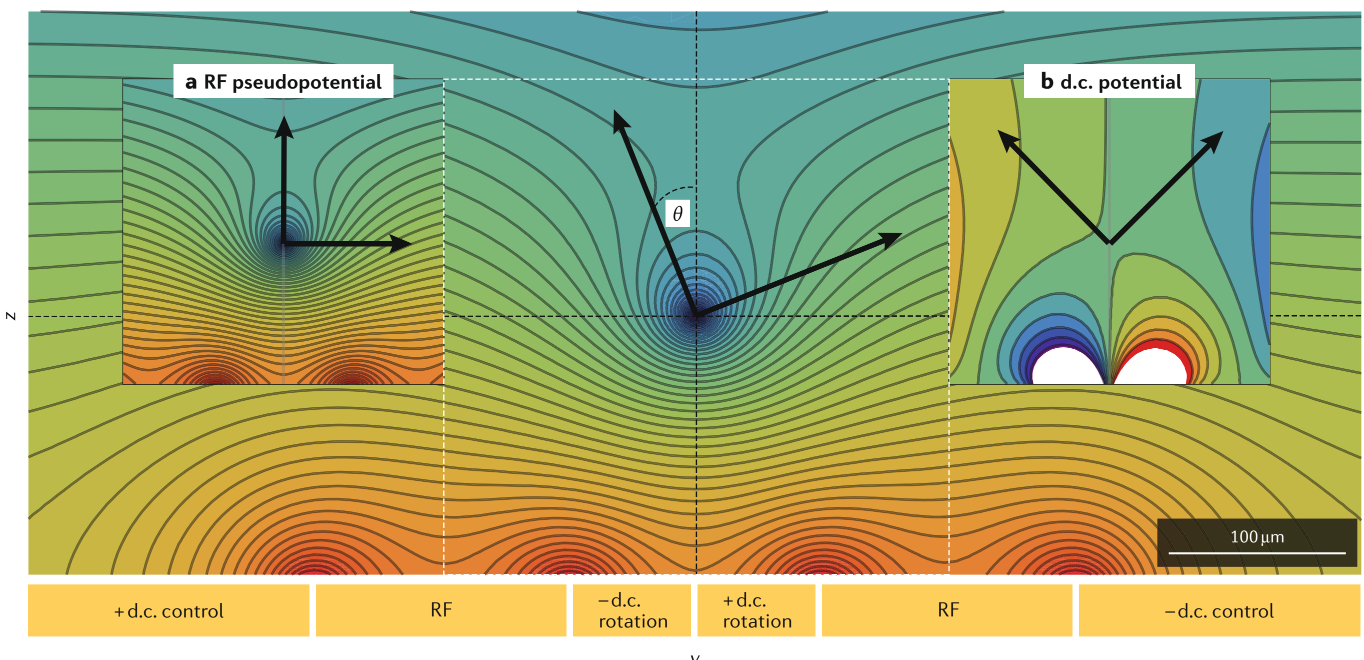


Fig. 1 | **Method of rotating the principal axis by angle θ using a six-wire surface trap design**[41]. The arrows indicate the principal axis in the radial directions. The relative sign of the voltage to achieve the rotation is indicated on the d.c. electrodes. The length scale indicates typical dimensions of the electrodes, but these can vastly differ depending on the desired ion height and trap parameters. The central contour plot shows the total potential, ϕ_{tot}, created from the superposition of the RF pseudopotential and the d.c. rotation potential created by asymmetric voltages on d.c. electrodes. **a** | The RF pseudopotential. **b** | The d.c. rotation potential. Blue and red contours indicate low and high potentials, respectively. The dashed white square indicates the corresponding regions of the two insets **a** and **b**.

'rotation' electrodes. Rotation electrodes can be introduced by replacing the central ground electrode in a five-wire geometry with two electrodes that occupy the same space, creating a six-wire geometry. As this will move the ion out of the RF nil, additional voltages are applied to the control electrodes (FIG. 1) and are required to compensate for non-zero fields[41,49]. Asymmetric RF electrodes were initially used for surface traps, until proposals were made to rotate the principal axes by using d.c. voltages instead. The use of asymmetric d.c. voltages applied to these electrodes became a popular approach since it could easily achieve an 'out-of-plane' principal axis angle of rotation of $\theta = 45°$, allowing for all degrees of freedom to be addressed by a planar laser path[41].

Design for ion transport and quantum simulation. Some applications, especially quantum computation, require the ability to move ions in a trapping potential such that certain operations are only performed on particular ions. In general, there are four types of operation required: linear shuttling, junction shuttling, and separation and combination of ion crystals. These operations are carried out by using time-dependent voltages applied to control electrodes located on the trap. The optimal geometries of these electrodes (in relation to electrode–ion distance) for operations such as linear shuttling and ion crystal (re)combination have been discussed elsewhere[43,47]. These transport operations have been reliably demonstrated with high fidelity[50–54], based on theoretical work[55–57].

Whereas linear shuttling operations can be performed using the types of ion traps previously discussed, junction shuttling and, by extension, ion trapping in 2D grids or planes require several modifications. Arrays of trapping zones arranged in a 2D plane were proposed in REF. 17 and expanded towards an industrial blueprint for quantum computing[19]. The realization of ion transport through a junction was demonstrated in a T-junction ion-trap array[58]. Subsequent studies identified optimal geometries for ion-trap arrays in which linear regions are connected to others through junction nodes[59,60]. At the centre of a junction node, three (T-junction[58] or Y-junction[61]) or four (X-junction[62]) branches of linear rails join together, making the assumption of an infinitely long rail no longer valid. Consequently, the uniform extension of the RF nil along the axial direction terminates at some point (FIG. 2). Changes in the ion's secular frequencies or the transport over a gradient in the pseudopotential, such as that caused by a junction, can lead to the motional heating of the ion[62,63]. To minimize these effects, optimized geometries have been introduced to improve junctions[60,64,65]. Most of these optimized geometries are created using iterative optimization methods such as a genetic algorithm. Through these designs, a number of successful experimental results of junction transport have been reported[61,62,66], achieving 10^5 consecutive transports with Doppler cooling and 65 without[64]. Furthermore, preservation of quantum information during trapped-ion transport has been demonstrated with 99.9994% state fidelity[54].

The previous designs are used for generic ion traps, but for quantum simulations 2D ion lattices of stationary

Fidelity
The reliability of a certain operation. For a fault-tolerant quantum computer, the fidelity of every single operation must be above the relevant fault-tolerant threshold (99%).

Node
An established fabrication method that uses fixed fabrication methods to create structures. These can be characterized by feature size, materials, voltages and many other aspects.

Pseudopotential
An effective potential that accounts for the ion's motion in an oscillating electric field.

Box 1 | **Ion-trapping basics**

The application of an RF voltage to the ion-trap electrodes creates a trapping potential. In addition, d.c. voltages produce a static field that confines the ion in the axial direction[1]. This can be expressed as

$$\varphi_{tot}(x,y,z,t)=\varphi_{d.c.}(x,y,z)+\varphi_{RF}(x,y,z)\cos(\Omega t), \quad (3)$$

where φ_{tot}, $\varphi_{d.c.}$ and φ_{RF} are the total, d.c. and RF potentials, respectively, and Ω is the frequency at which RF is being driven.

The equations of motion for a particle of mass m in a Paul trap are given by

$$\ddot{x}+\frac{e}{mr_0^2}\left(\varphi_{d.c.}-\varphi_{RF}\cos(\Omega t)\right)x=0.$$

where r_0 is the distance from the centre of the trap to the RF electrodes. These equations can be written in the form of the Mathieu equations

$$\frac{d^2 i}{d\zeta^2}+(a_i-2q_i\cos(2\zeta))i=0,$$

where a_i and q_i are the stability parameters in a direction i. Only a small subset of these parameters provide stable trapping. These are given by the Floquet theorem[147]. In the regime where $1>q_i>>a_i$, the ion's motion can be characterized in two ways: 'secular motion' and 'micromotion'. Secular motion is the motion due to the curvature of the electric potential. This motion is often used to implement coupling between spin and motion[148]. Micromotion is an often unwanted part of the ion's motion and can be split into two forms: intrinsic and extrinsic micromotion. The latter is caused when the ion is not in the RF nil (because of an external field contribution) and hence is subject to an additional, oscillatory component of motion. This can be compensated for by moving the ion to the RF nil. Intrinsic micromotion is the result of the ion's secular motion causing an effective offset of the RF nil in which the ion moves with an additional motion at the drive frequency Ω. This occurs even at the RF nil and cannot be compensated for entirely (see REF.[149] for a detailed discussion of micromotion).

ions (with small inter-site distances) can be beneficial. Ion traps to create these lattices have been successfully fabricated as mechanical structures[46], and subsequently as a microfabricated ion-trap chip[26]. A useful tool was introduced in REF.[67] for creating geometries required for close lattice sites. With this tool, lattice geometries have been fabricated with close, inter-site distance and multiple degrees of freedom per site[27,68]. The tool has also been used to investigate bi-layer ion traps that can be used to achieve stronger coupling between adjacent sites than with lattices fabricated on surface ion traps[69].

Numerical simulation tools. As the scope of ion-trap experiments has evolved, so have the requirements of the ion traps themselves. Such requirements include the introduction of vertical holes penetrating the substrate for additional access for laser light or atomic flux to the ion position[70], or the split rotation rails and the junction geometries already discussed before. For those geometries, analytical methods are no longer viable, and therefore numerical simulations of the electric fields are essential for designing electrodes. In the early days of surface traps, the boundary element method was used to simulate simple geometries, with a single electrode layer[71], owing to the limited computational resources available. Advances in computational power meant that the finite element method became a viable simulation tool. Geometries with greater complexity, including structures for schemes with oscillating magnetic field gradient, are routinely modelled and optimized using this method[65,72,73]. The X-junction device in FIG. 2 has been optimized to reduce the pseudopotential gradient, which, in turn, reduces the motional heating rate, $\dot{\bar{n}}$, during ion transport[64].

MEMS
Micro-electro-mechanical systems combine electrical and mechanical features in a fabricated device. The sizes of the features used often make the processing similar to ion traps.

CMOS
Complementary metal–oxide semiconductor is a material structure that is used to make digital logic circuits. This is a mature industry that produces highly reliable structures in high quantities.

Microfabrication techniques

The semiconductor industry revolutionized the creation of miniature electronic devices by using patterned conducting and insulating materials, the most common example being CMOS. Key to this success are highly reliable and reproducible processes using well-established fabrication facilities (foundries). Microfabricated ion traps have been made in such foundries[30,32]. However, some ion-trap-specific requirements necessitating structures that do not use established processes (such as formation and subsequent patterning of thick dielectric layers) or materials (such as gold and copper) are not possible in many foundries. As a result, modern ion-trap fabrication borrows techniques from different microfabrication technologies, such as MEMS, with the ultimate goal of achieving reproducible processes such as those used in CMOS. Problems of anomalous heating are addressed in BOX 4.

General considerations for microfabrication of ion-trap chips. Critical features that should be considered when designing ion-trap chip structures, and their required fabrication processes, are as follows.

- The electrodes should be able to sustain a RF voltage suitable for that ion species (heavier ions require larger voltages). A higher RF voltage allows trapping of ions further from the chip surface, reducing the effects of the electric field noise and laser scattering from the chip surface. In addition, higher voltages can allow higher trap depths and secular frequencies.
- Coupling of the RF field into the substrate should be minimized to prevent power loss and heating of the device[59].
- The area of dielectric exposed to the trapped ions should be minimized. In general, any dielectric should be sufficiently shielded such that electric fields from trapped charges on the dielectric are not felt by the ion. This is because factors such as ultraviolet (UV) lasers incident on dielectric surfaces can generate time-varying, stray charges in the dielectric[74–76], which in turn cause unwanted, time-dependent, ion displacements.
- All the materials, including various deposited films, should be compatible with ultra-high vacuum (UHV) environments. The chip should also be able to withstand processes required to achieve UHV such as baking and cryogenic temperatures.
- There must be unobstructed optical access between the laser sources, detectors and ions. This requires, for example, that wirebonds do not impede the optical path.
- Exposed surfaces should be contaminant-free to the greatest extent possible, to reduce the anomalous heating of ions[77,78]. In addition, a lower surface roughness reduces unwanted laser scattering and has also been suggested to reduce anomalous heating at cryogenic temperatures[79].

Substrate materials. Designing a fabrication process for ion-trap chips starts with the selection of layer materials, since the number and dimensions of thin film layers can greatly change the complexity of the entire process. Dielectric and conductive (or semiconductive) substrates have their own distinct advantages and disadvantages. Dielectric substrates allow a simple fabrication process and low power loss and heat in the substrate. However, accurate bulk micromachining of dielectric substrates for introducing vertical penetration holes and buried metal layers can be difficult. Another concern is that exposed dielectric surfaces can trap charges, causing stray electric fields[74].

Silicon is the most widely used material in modern semiconductor technology and has the advantage that it can be used in many processes that are not compatible with insulating substrates. It is, however, very lossy in the mid-range resistivity (10^2–$10^4\,\Omega$ cm) for RF frequencies[80]. To compensate for this, the simplest and most widely used method is to place an additional metal layer referred to as a 'ground plane' (M1, FIG. 3) between the RF electrode and the substrate. Although this adds complexities to the fabrication of silicon ion-trap chips, it is widely adopted as it almost guarantees the successful shielding of the substrate from RF dissipation. Another approach is to use substrates with either very high or very low resistivity[81]. In this case, the temperature dependence of the silicon resistivity should be considered: at cryogenic temperatures, silicon can even act as an insulator[82].

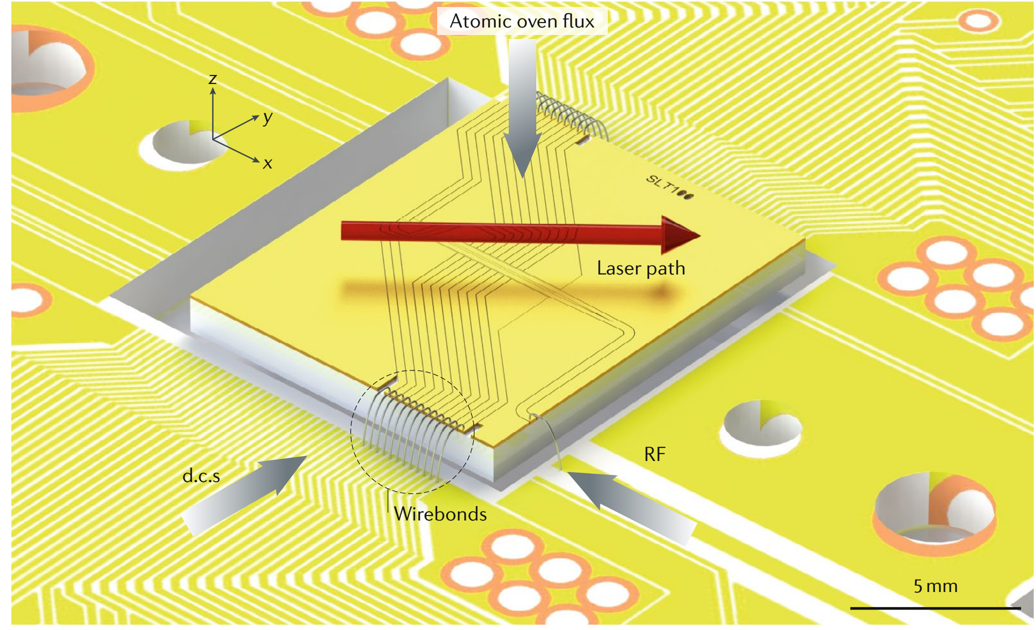
Standard fabrication processes for ion traps. A typical fabrication process for a silicon-based, surface ion-trap chip is shown in FIG. 3. The trap consists of a ground layer (M1), an electrode layer (M2), and two dielectric layers (D1 and D2) that are used to electrically isolate the conducting layers and the substrate. When using an insulating substrate, a simple ion trap can be created by using M2 only, and its formation is similar to that of M2 described in this section. The process starts with the deposition of a dielectric layer on the silicon substrate, which insulates the ground

Box 2 | **An ion-trap experimental setup**

In a typical experimental setup, the ions are trapped in an ultra-high vacuum (UHV) chamber with feedthroughs to connect the ion trap to supporting electronics and viewports for optical access. An atomic oven with a small aperture produces a flux of atoms parallel to the trap surface[150]; a laser ionizes the atoms[151]. The atomic flux can lead to unwanted surface coating, and many efforts have been made to reduce this, for example, by loading through a hole in the trap itself[61].

To initially cool the ions, Doppler cooling is used[152]. When Doppler cooling, all three directions of motion must be considered to effectively reduce the ion motion. To cool the in-plane directions of motion, the laser is typically positioned parallel to the surface, at a 45° angle with respect to the *x* and *y* directions of motion to have cooling components in both. The *z* motion can be effectively cooled by rotating the principal axis, using the methods discussed in the main text. Additional lasers and laser paths may be required to perform laser-based quantum logic operations[153].

An important consideration for ion trapping is optical access to the ions. Wirebonds are often used to connect the trap to a supporting printed circuit board. If the wirebonds are in the path of a laser, unwanted scattering will occur, which will seriously affect the ability to perform experiments. Scattering also occurs because of the divergence of a planar laser beam, scattering off the surface of the trap. Some surface ion traps have been especially developed to reduce this scattering by including an optical access hole that allows laser access through the trap[49]. To image the ion, external optics, combined with charged-coupled devices and photomultiplier tubes, are used. These sensors and optics are typically outside the vacuum system, but efforts are being made to integrate the required technology for the detection of ions into the ion-trap structure.



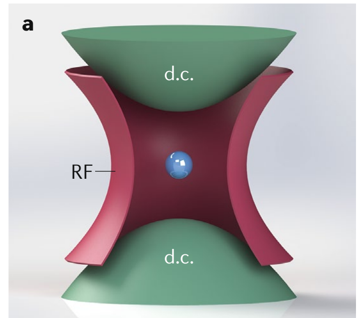
Box 3 | **Evolution of ion-trap structures**

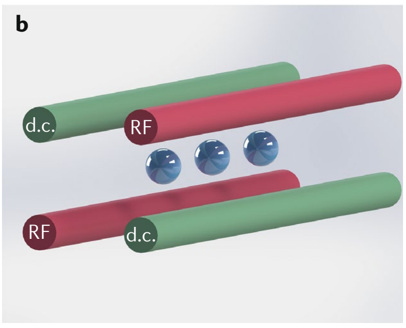
The first Paul trap (panel **a** of the figure) used hyperbolic electrodes in a 3D configuration[1]. With this structure, the isolation of a single ion[154] and the demonstration of a quantum logic gate[155] were performed. However, the structure could only trap a single ion without considerable micromotion, which limited the measurement accuracy of atomic resonances. To address this limitation, the linear Paul trap was developed[156,157]. These traps consist of four machined rods assembled in parallel to confine ions radially, and two end-cap electrodes to confine them axially[158] (figure, panel **b**). One of the most important characteristics of this linear trap is that ions in the same string share their motional modes.

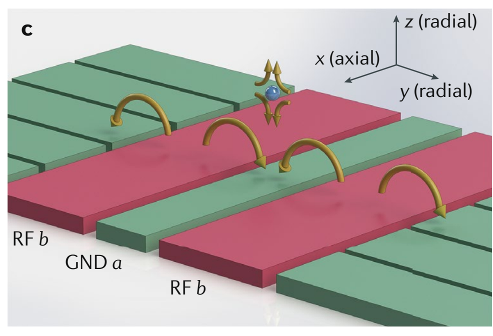
High voltages (>1 kV) can be applied to the four-rod trap, which allows the creation of deep trapping potentials while maintaining stable trapping parameters. The electrodes are sufficiently far from the ions to minimize the effects of electrical noise from the electrodes. Segmenting the rods allows axial control of the trapping potential, so these traps are used in experiments with ion chains in situations that do not require microfabricated devices[159–162].

Several quantum computing architectures[17,19,163,164] require reliable, reproducible devices and precise control over the ion's position, the latter being realized with more electrodes of smaller size. To address this, lithographic techniques from the semiconductor industry were used to fabricate ion traps[22,165]. These traps reproduced the four-rod structure on a micrometre scale, but the vertical distance between the electrodes was inevitably limited by the technical capability of thin-film processes. A solution was proposed[28] and subsequently demonstrated[23]: a direct projection of the rods onto a single plane, resulting in a five-wire geometry. This trap lays two RF electrodes and three ground (GND) electrodes alternately, as shown in the figure, panel **c**. Here *a* and *b* represent the widths of the ground and RF electrodes respectively, and the yellow arrows indicate the electric field when the RF electrode has a positive voltage applied. This chip structure is referred to as a surface electrode trap (or surface trap) and has become the most widely used geometry for microfabricated ion-trap chips.

Advances in fabrication technologies have allowed more complex designs to be pursued[17,26,27,29,61].







plane from the substrate. A 1–2 μm layer of either SiO_2 or SiN_x is used for this and is typically grown by plasma-enhanced chemical vapour deposition or as a thermal oxide. A ground plane, M1, is deposited on the D1 layer (FIG. 3) using any UHV-compatible conductive material such as Au, Al or Cu. This is commonly a layer 1–2 μm thick, either sputtered or evaporated onto the device. When developing chips with vertical interconnect access ('vias') to improve electrode routing, these thin insulating and conducting layers can be stacked multiple times[83]. Since high RF voltages applied between the electrodes and ground plane are desirable in surface ion traps, the D2 layer separating the two metal layers should be thick to maximize the voltage at which electrical breakdown occurs. Thus, the thickness of the D2 layer is generally of the order of 10 μm, with the deposition and etching of this layer usually being the most difficult steps throughout the entire ion-trap fabrication process (FIG. 3). This is because such vertical dimensions are generally not covered by conventional semiconductor processes, which also limits the material choice for the dielectric layer to plasma-enhanced chemical vapour deposition SiO_2 or SiN_x. A polymer-based, spin-on dielectric has been demonstrated[84] for ion-trap fabrication, which allowed for thick dielectric layers. The deposition of the top metal layer (M2) can be performed by using conventional microfabrication processes including electroplating, sputtering and evaporation (FIG. 3), and can be patterned using plasma dry-etching (FIG. 3). Because the top layer is directly exposed to the trapped ions, more factors should be considered when selecting the electrode material. Gold is one of the most widely used materials for the top metal layer, owing to its extremely low oxidation rate. However, since gold is not compatible with many conventional microfabrication techniques, a thin gold layer can be deposited on aluminium electrodes as a final step[85]. The final step etches the dielectric layer in both the vertical and lateral directions to reduce the effect of charges trapped on the dielectric surface. The vertical etching of the thick dielectric layer (FIG. 3) uses the electrode pattern as a mask, and reactive ion etching. This is followed by isotropic wet or gas etching of the dielectric sidewalls (FIG. 3), which helps to minimize the exposure of the ions to trapped charges[49].

The fabrication methods described here are commonly used to create a silicon-based ion-trap chip. Microfabricated ion traps can also be made by many different, additional processes not discussed in this Technical Review[35,38]. Furthermore, fabrication processes have been optimized for specific capabilities, such as extremely high breakdown voltage[26,86], or entire shielding of dielectric sidewalls[76]. 3D quadrupole traps have also been fabricated with new techniques that allow large ion–electrode distances (hence low motional heating rate) for a lower trap drive voltage than surface ion traps[29,87]. The use of a transparent material, indium tin oxide (ITO), as the electrode layer allowed detection of fluorescence emitted from ions with a photodetector underneath the electrode on the backside of the trap chip[88]. A selection of microfabricated ion traps, which includes both surface and 3D quadrupole traps, is shown in FIG. 3.

To integrate various on-chip features, post- or pre-processing steps can be added to the fabrication

Plasma-enhanced chemical vapour deposition
A method of depositing materials through chemical reaction of ionized gases.

Breakdown
The point at which two electrically isolated electrodes become shorted because of a large voltage, often damaging the electrodes in the process.

Sputtering
A method of depositing a variety of materials onto a surface using accelerated ions striking a target of the desired material.

Evaporation
A method of depositing metals onto a surface by evaporating a metal and allowing the resulting flux to coat the surface.

Reactive ion etching
Also known as plasma etching, a method that uses a plasma to directionally etch a material.

CCWs
Current-carrying wires are ion-trap-specific structures that are designed to use currents to generate magnetic fields.

Damascene process
A fabrication process in which a pattern is etched that is subsequently filled (such as with copper). It is then planarized using a chemical mechanical polish. The dual damascene process combines pattern and vertical connections into one fabrication process.

flow of the basic ion-trap structures described previously. As an example of post-processing, a vertical slot penetrating the silicon substrate can be fabricated by a conventional deep silicon etching process at the end of ion-trap fabrication. This hole can be used to load neutral atoms[89] or to provide increased optical access[90]. For the integration of optical or electrical devices, the ion trap is fabricated on top of pre-processed wafers where the integrated feature has already been fabricated. This inevitably introduces restrictions on the processes and materials used, so these concerns should be addressed to ensure cross-compatibility between fabrications. For ion traps that use multiple integrated technologies, compatibility between processes can be an extremely difficult problem to solve and is likely to become a strong focus of the ion-trap community.

Advanced on-chip features

As ion-trap geometries become more complex, either for quantum simulation or scalable quantum computation purposes, supporting systems are often required to sit within the footprint of the ion-trap device[19]. Examples include integrating optical and electrical devices used in experiments into the microchip. These approaches can also contribute to the miniaturization of precise measurement devices such as atomic clocks and mass spectrometers, combined with efforts to miniaturize vacuum chambers[24,34]. This section mainly discusses research into chip-level integration of advanced features. Several of the processes for advanced feature integration use fabrication methods or materials that are not covered in this Technical Review. Readers are invited to see the referenced material to learn about the extensive and varied processes as required.

Embedded gate schemes. Several schemes for implementing quantum logic gates between qubits rely on magnetic field gradients, either static[91,92] or oscillating[93,94]. Three methods have been used to create the gradient: permanent magnets, placed near the trap to produce a static gradient at the ion position[92,95–97]; in-plane current-carrying wires (CCWs), fabricated as part of the electrode layer, which allow the creation of both static and oscillating magnetic field gradients[72,98–100]; and sub-surface CCWs, fabricated below the electrode and ground plane layers[101].

Permanent magnets are commonly used for the static gradient scheme, achieving gradients of up to 36 T m^{-1} (REF.[97]). Scaling up to large systems may prove difficult due to the need for a careful, manual alignment of the ion trap to the magnets.

In-plane CCWs have been shown to provide oscillating gradients of up to 54.8 T m^{-1} (REF.[73]). In this scheme, the trap geometry must be altered to accommodate the CCWs, and the power dissipation must be considered. The power dissipation could be reduced by using thicker layers, to decrease resistance, but the skin depth of the oscillating field in the electrodes may quickly limit this, depending on the transition required and electrode material.

Sub-surface CCWs, situated beneath the ion trap, do not impinge on the electrode design and can be used for both static and oscillating gradients. For the latter, the field is likely to be attenuated owing to shielding induced by currents in the ion-trap electrodes and ground plane layers. One such device[101] used Cu wires 127 μm thick, fixed to an aluminium nitride chip carrier and mounted 285 μm below the trap surface. A gradient of 16 T m^{-1} was achieved by using a current of 8.4 A.

Larger gradients could be achieved with sub-surface CCWs by reducing the wire-to-ion distance. It has been suggested[19] that the CCWs could be embedded into the substrate surface, using the dual damascene process, and the ion trap fabricated directly above the wires. By embedding the CCWs into the substrate, not only is the trap-to-wire distance decreased, but thermal sinking is improved. Thus, greater current, and higher gradients, should be feasible[19]. Our group has already demonstrated the application of a current of 11 A (corresponding to a current density of 10^{6} A cm^{-2}) to an ion microchip, which should result in a magnetic field gradient of >185 T m^{-1} at an ion height of 125 μm. At an ion height of 40 μm, this method is expected to produce a gradient in excess of 1,000 T m^{-1} or conversely obtain ~185 T m^{-1} with much lower current required (~3 A).

Although a relatively new technology for ion traps, CCWs are commonplace in the atom-trapping community, where large, steep magnetic fields are used to trap neutral systems[102–105]. The currents and wire dimensions used for atom trapping are similar to those required by trapped-ion gate schemes, and therefore much of what has been learned in the atom-trapping field may also be applicable.

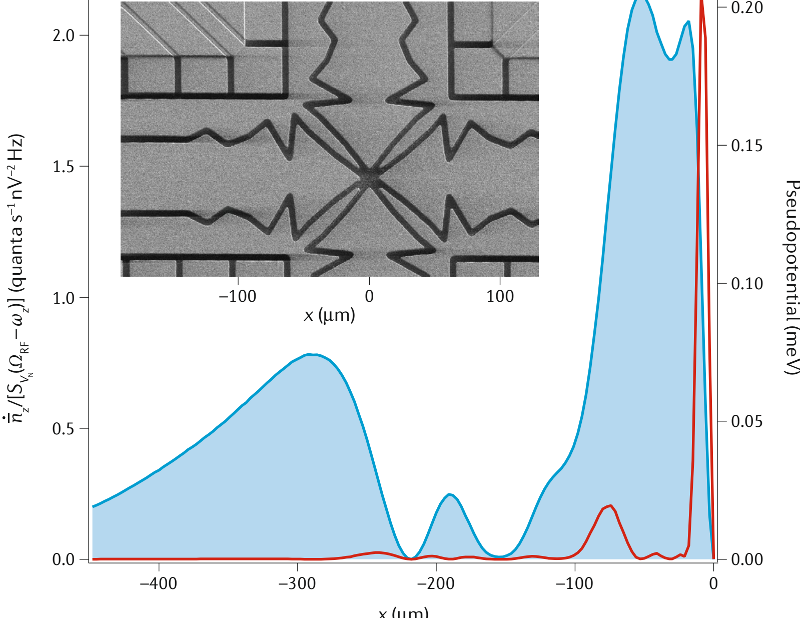
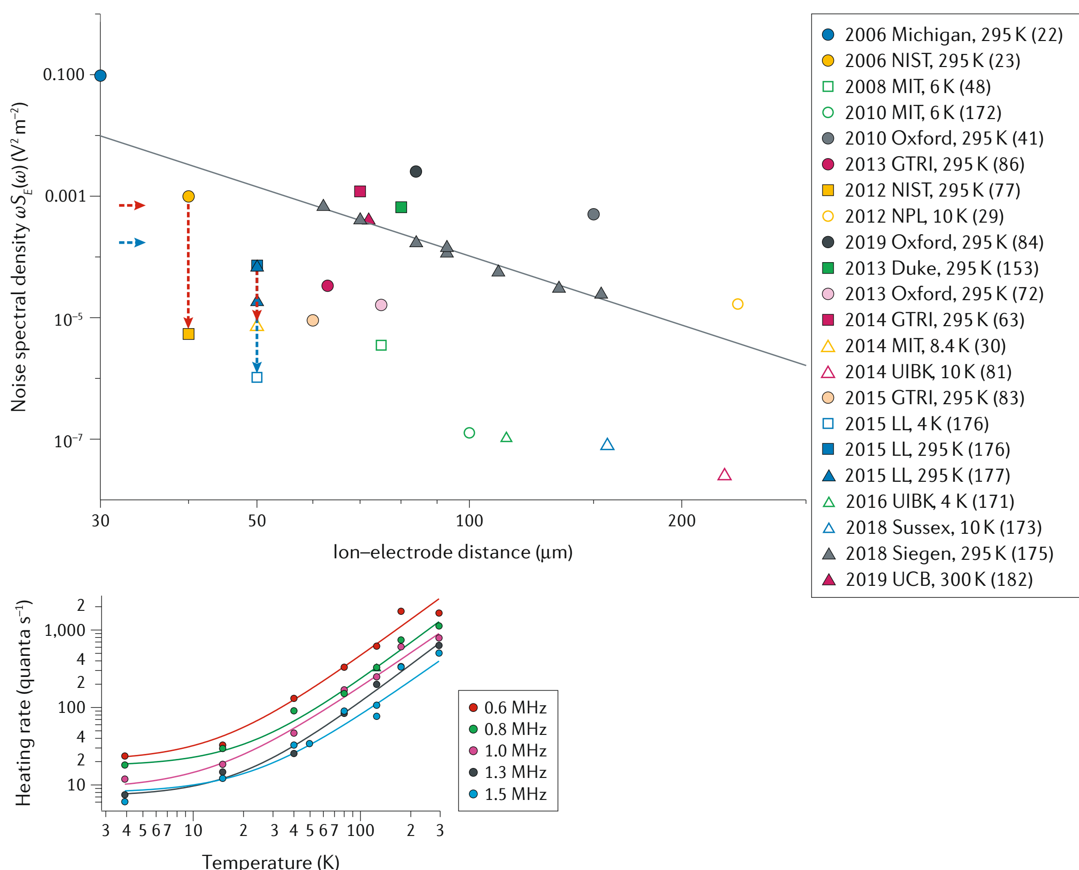


Fig. 2 | **X-junction electrode geometry.** The geometry is optimized at the junction centre (inset image) to reduce the ratio of the motional heating, $\dot{\bar{n}}$, to the spectral voltage noise, S_{V_N}, which is expressed as the quantity $\dot{\bar{n}}/S_{V_N}$ (red line) to normalize against material- and electronics-dependent noise. This ratio provides a measure of the gradient in the pseudopotential and local secular frequency, both of which determine the motional heating during ion transport[62]. The blue shaded line shows the RF pseudopotential along the transport direction. The trap potential is calculated for a ^{40}Ca ion with $V = 91\,V_{rms}$ and $\Omega = 2\pi \times 58.55$ MHz. Adapted from REF.[64], CC BY 3.0.

Box 4 | **Efforts to deal with heating rates**

Despite many successful implementations of surface traps, miniaturizing the ion-trap structure has also created a number of side effects, one being the 'anomalous heating' of the trapped ions[21]. This is thought to be induced by electric field noise from the surface of the trap electrodes. The electric field noise can couple to the ion motion when the frequency is near the motional frequency of the ion. This in turn leads to an increase in the phonon number, which is detrimental to the implementation of quantum logic operations. Many efforts have been made to investigate this heating, both theoretically[166,167] and experimentally[168–173]. One method of reducing the heating rate is to increase the distance, d, between the ions and the electrode surface, since it has been experimentally shown that the heating rate scales approximately as d^{-4} (REFS[169,174,175]). However, given that the maximum voltage that can be applied to a trap chip is limited by current semiconductor technologies, an increased distance inevitably leads to a shallower trap depth, so there is a limit to how much d can be increased. Another method to reduce the heating rate is by cooling the ion trap to cryogenic temperatures, as demonstrated in REF.[169]. This approach can reduce the heating rate by two orders of magnitude[48,169,176]. Other approaches use in-situ cleaning of the chip surface[77,177]. Since hydrocarbon-based contaminants adsorbed on the electrode surface during the bake-out process are suspected to be a major source of the electrical noise that induces anomalous heating[178], removal of these contaminants after bake-out can also reduce the heating rate by two orders of magnitude. Owing to these efforts, extremely low heating rates of ions have been reported[81]. More work is under way to better understand the source of anomalous heating[179–184].

The figure summarizes the heating rates in microfabricated ion traps as a function of ion–electrode distance. The measurement results of heating rates are expressed as noise spectral density with a fit line demonstrating a heating-rate scaling of $d^{-3.79}$ (REF.[175]). The heating rates measured in a cryogenic environment (open points) are noticeably lower than those in room-temperature systems (filled points). The red and blue arrows indicate the changes made in the same experimental setup by in-situ surface cleaning and cryogenic cooling, respectively. The lower panel shows the temperature dependence of the heating rate, showing significant gains from room temperature to cryogenic temperatures. Duke, Duke University; GTRI, Georgia Tech Research Institute; LL, Lincoln Laboratory, MIT; Michigan, Michigan State University; MIT, Massachusetts Institute of Technology; NIST, National Institute of Standards and Technology; NPL, National Physics Laboratory; Oxford, University of Oxford; Siegen, University of Siegen; Sussex, University of Sussex; UCB, University of California, Berkeley; UIBK, University of Innsbruck. Lower panel reprinted with permission from REF.[176], APS.



Optical components. For many trapped-ion technologies, addressing and state readout of ions is required using optical techniques on an individual ion basis. It is sometimes beneficial that such optical components are integrated into the device, to increase the fidelity of addressing and readout operations.

Optical fibres have many uses in trapped-ion experiments for both addressing and readout operations.

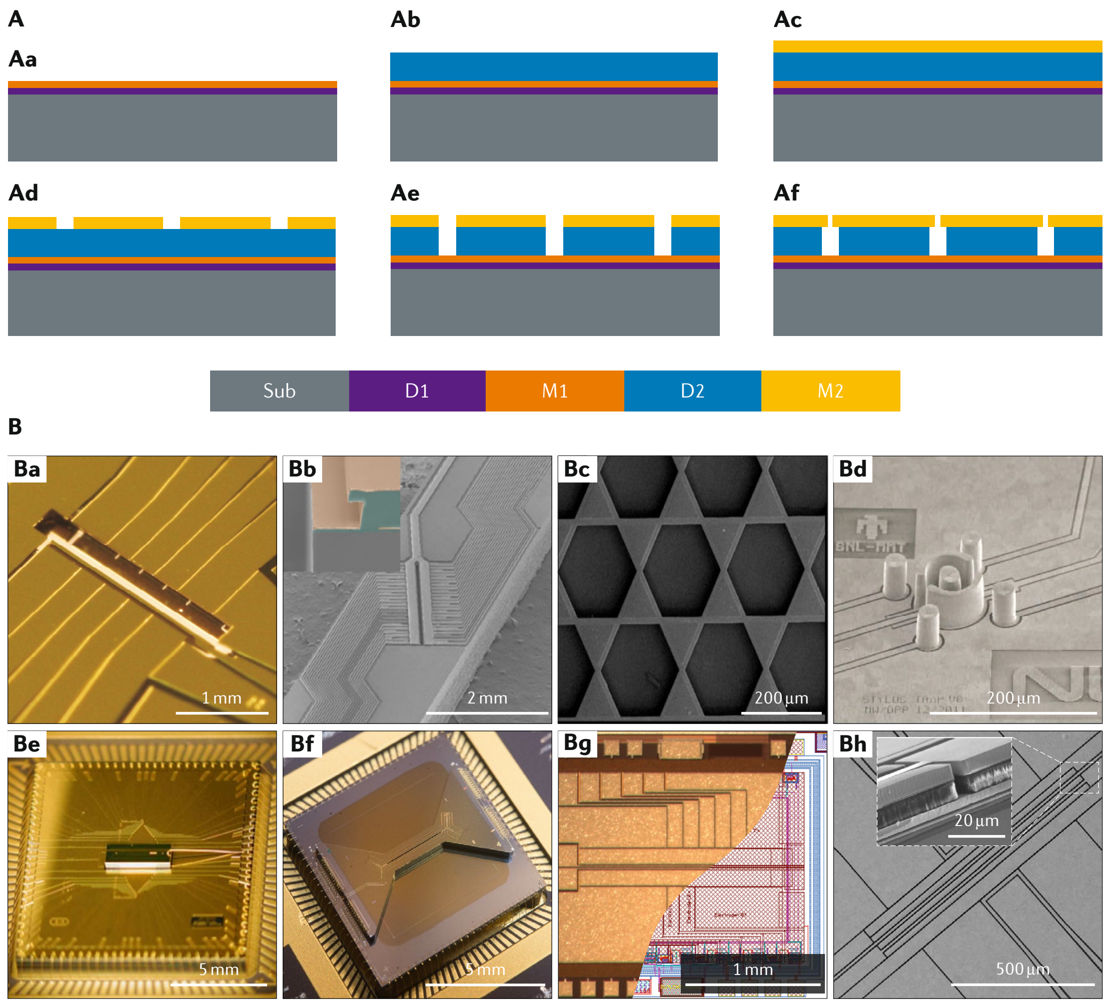


Fig. 3 | **Ion-trap chips. A** | Conventional fabrication process flow for a surface ion-trap chip. **Aa** | Forming a ground plane and an insulating layer (D1) that isolates the ground plane (M1) and the substrate (Sub). **Ab** | Deposition of a thick (micrometre-scale) dielectric layer (D2). **Ac** | Forming a metal layer (M2) on the dielectric. **Ad** | Etching of the metal layer (M2) to define the electrode patterns. **Ae** | Subsequent etching of the thick dielectric layer (D2). **Af** | Isotropic etching of the dielectric pillars from the sidewalls to reduce the area of dielectric sidewalls exposed to the ion. **B** | Images of various ion traps. **Ba** | Microfabricated 3D quadrupole trap. National Physics Laboratory. **Bb** | Low dielectric exposure. Seoul National University. **Bc** | 2D array on a chip featuring a high breakdown voltage. University of Sussex. **Bd** | Large metal structures. National Instituite of Standards and Technology. **Be** | Through silicon via (TSV) in an ion trap .GTRI/Honeywell. **Bf** | High optical access. Sandia National Laboratory[61]. **Bg** | Ion trap fabricated in a CMOS foundry. Massachusetts Institute of Technology. **Bh** | New fabrication method for thick metal/dielectric layers. Physikalisch-Technische Bundesanstalt. Part **Ba** adapted from REF.[29], Springer Nature Limited. Part **Bb** adapted with permission from REF.[76], IEEE. Part **Bc** adapted from REF.[6], Springer Nature Limited. Part **Bd** adapted with permission from REF.[146], AIP Publishing. Part **Be** adapted with permission from REF.[83], AIP Publishing. Part **Bf** adapted with permission from REF.[42], © National Technology and Engineering Solutions of Sandia, LLC. Part **Bg** adapted with permission from REF.[32], APS. Part **Bh** adapted with permission from REF.[84] CC BY 3.0.

The typical structure of a fibre, however, is not naturally suited to an ion-trapping experiment, as an exposed dielectric near the ion can disturb the trapping field. By integrating an optical access hole, the dielectric can be shielded by the ion trap itself, allowing fibres to be brought close to the ion[70,90,106].

To address multiple ions, integrating optical waveguides into the ion trap is a promising way forward. A multi-ion addressing technique has been demonstrated[107,108] that uses integrated silicon nitride waveguides and grating couplers to address individual ions, with a total optical system loss of 33 dB. Using integrated waveguides[109], light of multiple wavelengths was delivered to a trapped ion. This demonstration was combined with packaging methods that allowed a direct optical fibre attachment to the waveguides. Through these methods, a single-qubit gate with a $^{88}Sr^{+}$ ion was performed with 99% fidelity[108] and, more recently, two-qubit gates with $^{40}Ca^{+}$ were demonstrated[110]. Another approach for the scalable laser addressing is to adjust beam paths with electrically controlled devices. Controlled beam steering with MEMS mirrors has been demonstrated[111], but this technology has yet to be integrated into a trap.

Integrating mirrors into the ion-trap surface can allow more photons from the ion to be collected, by

Collection efficiency
The percentage of collected photons that have been emitted by an object.

Numerical aperture
A value that characterizes the solid angle over which a sensor or light source is exposed to an object, in this case an ion. This is a dimensionless quantity.

Die
A cut-out piece of a larger, fabricated wafer. For integrated circuits, a die is typically packaged in epoxy afterwards, making the circuits incompatible with ultra-high-vacuum environments.

reflecting otherwise lost photons. In REF.[112] micro-mirrors were integrated into a surface ion trap, enhancing photon collection of $^{40}Ca^{+}$ ion by 90%, which resulted in a collection efficiency of 14% (numerical aperture of 0.69). The experiment in REF.[113] used integrated diffractive mirrors to produce a 4.1(6)% coupling of the fluorescence from a $^{174}Yb^{+}$ ion into a single mode fibre, which nearly tripled the bulk optics efficiency. Integrated mirrors can also be used to create cavities on chip, for instance to facilitate atom–light coupling for photonic interconnects. Towards this endeavour, ion traps have been fabricated on top of high-finesse optical mirrors to create a cavity[114,115]. However, more development is needed before strong coupling, already demonstrated macroscopically[116], can be achieved in such a microfabricated device.

Standard ion-trapping detection uses large collection optics, which help to counteract the effect of being outside the vacuum system and hence further from the ion[117]. By integrating a detector into the actual trap chip, the detector–ion distance decreases, which could help in capturing more photons with appropriate optics in place. Studies have suggested[19,118] using integrated single-photon avalanche diodes (SPADs) for light detection. A transparent trap made of ITO with an integrated photodetector featured a collection efficiency approaching 50%[88]. Another work[31] showed UV-sensitive superconducting nanowire single-photon detectors (SNSPD) made of MoSi, integrated into a microfabricated ion trap. This device demonstrated a detector fidelity of 76(4)% at a wavelength of 315 nm with a background count rate below 1 count per second. The trapping field decreased the system detection efficiency by 9%, but did not increase background count rates. Being a superconducting device, however, the stringent requirement for low operating temperature (3.2 K) introduces additional challenges, depending on the application. The use of SPADs, however, only requires temperatures of 70 K to achieve a performance similar to that of a photomultiplier tube[19].

Passive components. Capacitors, resistors and inductors are a key part of any ion-trapping experiment in filtering, resonators and general electronics[24,85,119,120]. Bringing these devices on-chip can have many benefits, from increased density of components to reduced noise because of the proximity to the device.

One method for high-density integration of passive components takes advantage of advanced CMOS facilities by incorporating a CMOS die. One example of this[33] integrated a 12-channel, bare-die *RC* filter array (35 kΩ, 220 pF) onto a printed circuit board. To attach the die, a standard low-outgassing silver epoxy was used, and channels were connected using wirebonds. Although not integrated on chip, the attachment methods are similar to those used by industry on silicon dies; hence, dies could be integrated on an ion trap if required. Using methods available at modern CMOS facilities[32] and careful calibration, one could realistically fabricate resistive temperature probes in the trap. Conversely, a resistive strip could act as a local heater for use in cryogenic systems to prevent gas molecules freezing out on the trap during cool down[81].

Capacitors can be fabricated into the trap with two metal planes separated by a dielectric. Trench capacitors take advantage of an increased surface area by etching vertically into silicon using well-established processes. This allows a substantial increase in the capacitance per unit area. For ion traps, this was achieved in REF.[85] where trench capacitors were integrated into the trap, which allowed 1 nF to be achieved in a 100 μm square. This was 30 times higher than the capacitance allowed in the same area when using a conventional, planar, fabrication process. A capacitive divider is a common method for measuring the large RF voltage applied to the ion trap[86]. Such a component could be integrated into the device itself using the methods discussed previously.

To create the low-noise, high-voltage RF trapping field, a helical resonator is commonly used[120,121]. This component relies on the ability to impedance-match using inductors. Efforts have been made to reduce the bulky nature of the device to a more manageable size[122,123], but integration is yet to be achieved. Microfabricated inductors[124] could be one route forward. For future devices, microfabricated inductors could also be used to replace the standard low-pass filter[85] with more advanced filters, such as a band-stop filter, to remove noise on d.c. electrodes.

Active components. In analogy with Rent's rule[125], it was suggested that for quantum computation, the scaling of interconnections and control lines with the number of qubits would become a major bottleneck[126]. This connectivity problem naturally led to the introduction of active components into the vacuum system[33], or even into the ion trap[32]. One of the key requirements for ion trapping is that all integrated components must be UHV-compatible[127]. This often eliminates the use of packaged electronics, making bare die a UHV-compatible alternative. Packaged components can sometimes be used when operating at cryogenic temperatures. In REF.[33], two 40-channel DACs (AD5370) were introduced into a UHV environment. For this experiment, the AD5370 was not sourced in bare-die form, but instead a standard, packaged, AD5370 was used and then decapsulated using nitric and sulfuric acids[128]. The assembly is as discussed in the next section. This is a new method to overcome the low supply of bare-die products, but it is likely that future devices using this technology would already be in bare-die form, hence suitable for UHV.

In REF.[32], a custom, CMOS DAC was integrated into an ion trap. The custom DAC was designed for the CMHV7SF 180 nm node from Global Foundries. Key to this node is the ability to allow for higher voltages (20 V span) compared with a typical <5 V span, thus allowing the implementation of an amplifier for voltages more suited for ion trapping. A switching device was also included to disconnect the ion trap from the DAC when not updating, hence reducing noise when disconnected. Since the electrode acts as a capacitor with low leakage current, the switch can disconnect the DAC while the electrode holds a voltage. The ion trap on top was also fabricated as part of the CMOS process, similar to that used in REF.[30]. A common concern with semiconductor

Ball-grid array
A method that uses raised metal balls/bumps to attach a die to a circuit.

devices is the 'freeze-out' at low temperatures, where the energy required to overcome a bandgap becomes too large. However, the previously mentioned device was operated at cryogenic (4 K) temperatures[32]. More complicated devices, such as a field programmable gate array (FPGA), have also been shown to work at such temperatures[129].

Stacked wafer technology. It has been proposed that backside connections to the ion trap will be required for a large-scale quantum computer to connect to its supporting systems[83]. This has been expanded[19] to use the wafer stacking of different components, such as DACs, detectors and cooling. These proposals require the introduction of through-substrate-via technology, often known as through-silicon vias (TSVs). These technologies have been demonstrated in ion traps by connecting an ion trap through a backside ball-grid array and TSVs[83] . In this work[83], the ion-trap die was attached using a ball-bonding method, which uses a programmed gold ball bonder to leave individual short, gold studs on an interposer. A localized eutectic bond was then used to connect the interposer to the back of the device. For wafer-scale bonding, issues occur with high stress (due to the device size) reducing the connection quality[130]. On a wafer scale, the studs are commonly microfabricated, as opposed to using a ball bonder[131]. Eutectic bonding is also not the only option for wafer-scale attaches; many other commonly used methods exist[132,133].

It has been suggested[19] that the microchannel cooling could be implemented as part of the stacked wafer proposal. This could also be used in other architectures, either for power dissipation or to reduce heating rates. Although they have yet to be introduced into ion traps, microchannel coolers have started to emerge for room-temperature devices capable of removing >300 W cm^{-2} (REF.[134]). A microchannel cooler using liquid nitrogen was capable of removing 1,000 W cm^{-2} (REF.[135]), helped considerably by an order-of-magnitude increase in thermal conductivity of silicon at ~70 K (REF.[136]). Difficulties with this design may emerge from the heat flow between the stacked wafer levels, and work is still required to develop heat-flow mechanisms between the wafers.

Outlook

Much progress has been made in the past 10 years on the development of complex microfabricated ion traps. Although the creation of custom potentials through simulations is well understood, unanswered questions still remain in terms of the integration of advanced technologies. A summary of the requirements for many different advanced ion traps is illustrated in FIG. 4. With most of these technologies having already been individually demonstrated in trapped-ion experiments, the microfabricated ion trap is expected to become a fundamental component for many quantum technologies.

Commercial realization of quantum technologies requires the large-scale fabrication of devices, with high reliability and yields. Many of the proposed technologies discussed in this Technical Review will require CMOS devices integrated into the ion trap. However, unlike the standard operation environment of CMOS, ion traps are often required to work at cryogenic temperatures. Whereas the development of cryogenic control electronics is also a priority for superconducting qubit platforms[137] and solid-state qubits[138], temperature requirements for ion-trap devices are much less stringent, only requiring operation at 70 K, or possibly 4 K where high cooling powers are available. Cryogenic CMOS integration of a DAC has recently been demonstrated[32] that already has the capability to be mass-produced. Although commercialized SNSPDs are relatively uncommon, SPADs are becoming increasingly widespread, with high demand from the driverless car market. SNSPDs may prove simpler to integrate, as they can be fabricated as part of the ion trap; however, they have to be operated at superconducting temperatures. Waveguide-on-chip technology is a developing field with many applications across the spectrum of quantum technologies. As a result, several fabrication facilities have appeared in the past few years that can offer some of the commercial capabilities required for the optical components discussed. Further development is still needed in this field to create optical components with greater suitability for blue and near-UV wavelengths and to introduce such components to an industrial-scale process. Wafer stacking and TSVs, while nascent technologies, are becoming prevalent in many different modern devices, such as high-bandwidth memory[139], and are well-understood processes[140]. Cooling requirements will become increasingly important considerations when integrating different technologies. Microchannel coolers provide a promising path towards managing the potential thermal requirements, but they have yet to reach the market.

Although fabrication and assembly industries allow individual aspects of an ion trap to be demonstrated, combining these technologies will be essential for creating more advanced ion traps. Separating the technologies on a wafer-by-wafer level may prove prudent in reducing risks of compatibility, but introduces new issues with inter-wafer connectivity for large devices and heat flow. Although integrating electronics can reduce some of the noise, thanks to the proximity of the supporting electronics and hence less 'pick-up', it can introduce new noise spectra owing to the integration of active components. This can be mitigated by additional filtering and noise manipulation to move the noise spectrum to frequencies that do not affect the ion. Some of the optical technologies discussed in this Technical Review will perform optimally only at certain wavelengths. Integrating many of these optical components could therefore require multi-species schemes to take advantage of these technologies[141–145]. With a wide variety of technologies being simultaneously integrated, unforeseen consequences are likely, so full integration will remain a tremendous engineering challenge.

Conclusion

Trapped ions constitute an extremely powerful system to realize and control quantum phenomena such as entanglement and superposition, showcasing

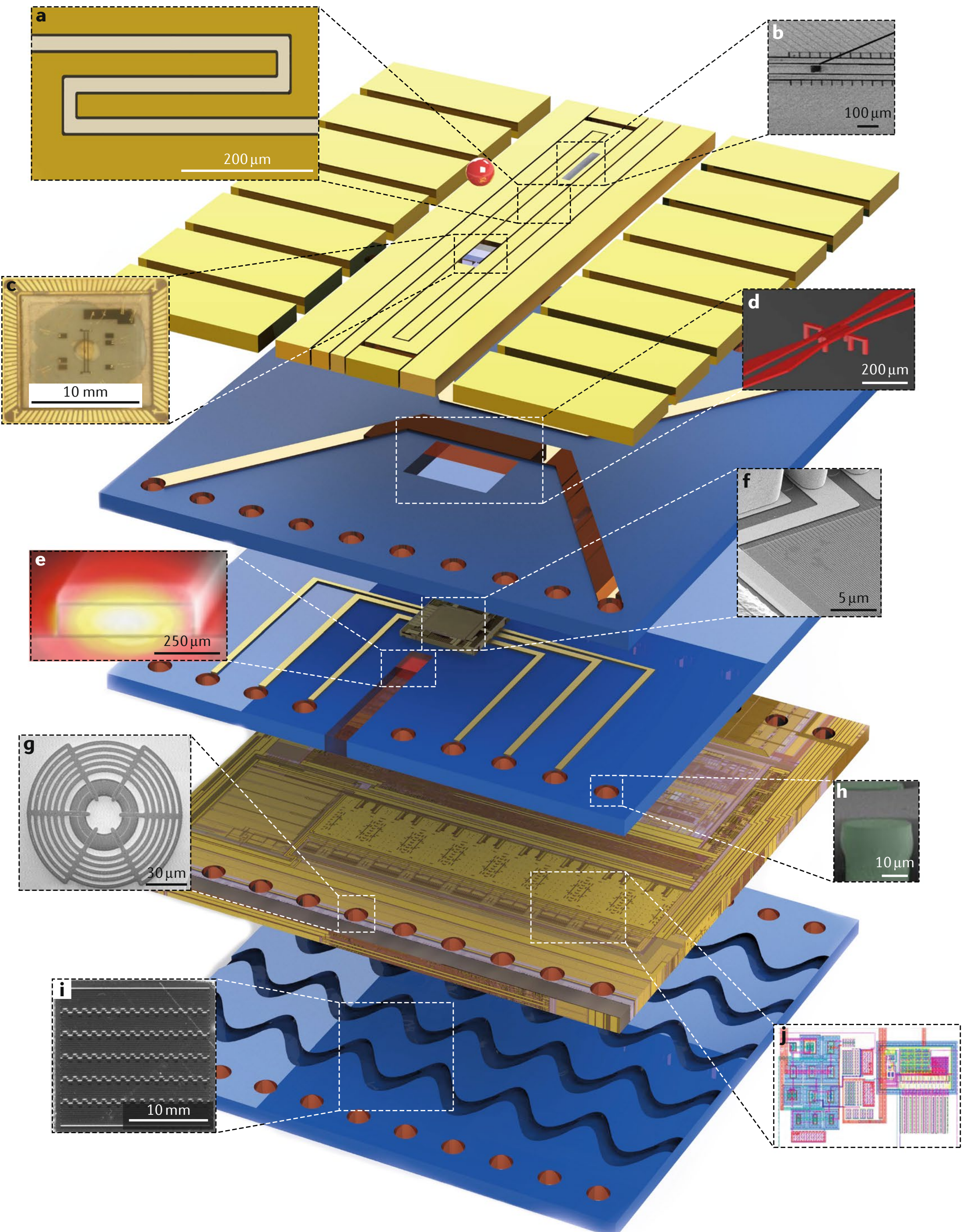


Fig. 4 | **Advanced on-chip technology in an ion trap.** Not all features are necessarily required, and their inclusion depends on the intended application. **a** | Oscillating-gradient current-carrying wires (CCWs). **b** | Backside loading. **c** | Transparent indium tin oxide (ITO) electrode. **d** | Static-gradient CCWs. **e** | Si_3N_4 waveguide and grating for individual optical addressing. **f** | Integrated photon detector. **g** | Trench capacitors. **h** | Through-silicon vias (TSVs). **i** | Microchannel cooling. **j** | Integrated electronics. Part **a** adapted from REF.[99], Springer Nature Limited. Part **b** adapted from REF.[64], CC BY 3.0. Part **c** adapted with permission from REF.[88], AIP Publishing. Part **d** adapted from REF.[19], CC BY 4.0. Part **e** adapted from REF.[108], CC BY 4.0. Part **f** adapted with permission from REF.[31], OSA. Parts **g** and **h** adapted with permission from REF.[83], AIP Publishing. Part **i** adapted with permission from REF.[134], IEEE. Part **j** adapted with permission from REF.[32], APS.

unmatched fidelities and coherence times. The emergence of ion microchips allows us to incorporate the advantages of modern microfabrication and microprocessor advances into this system, giving rise to a fully scalable hardware platform for a wide range of quantum technologies.

Published online 27 May 2020

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Acknowledgements
This work is supported by the UK Engineering and Physical Sciences Research Council via the EPSRC Hub in Quantum Computing and Simulation (EP/T001062/1), the UK Quantum Technology hub for Networked Quantum Information Technologies (no. EP/M013243/1), the European Commission's Horizon-2020 Flagship on Quantum Technologies Project no. 820314 (MicroQC), the US Army Research Office under contract no. W911NF-14-2-0106, the Fonds National de la Recherche Luxembourg (National Research Fund) Project Code 11615035 and the University of Sussex.

Author contributions
The authors contributed equally to all aspects of the article.

Competing interests
The authors declare no competing interests.

Peer review information
Nature Reviews Physics thanks Roee Ozeri and the other anonymous reviewers for their contribution to the peer review of this work.

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