Microfabricated ion traps for quantum information and simulation

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Introduction

The design and implementation of scalable ion trap fabrication methods is of key importance for ion trap quantum computing. A scalable ion trap quantum computer will require hundreds to thousands of control electrodes. Building such traps using conventional machining and assembly is a daunting if not impossible task and only realistic if microfabrication can be successfully harnessed to construct microfabricated ion trap arrays. This will allow large trap arrays to be produced without manual assembly and with higher levels of precision.

Currently several challenges face the implementation of microfabricated ion traps:
- Exposed dielectrics (uncontrollable static fields)
- Limited rf voltage (reduce trap depth and secular frequencies)
- Large ion heating rates.
- Geometries may not allow adiabatic transport
- Ability to scale

Here we show work towards overcoming these challenges.

Silicon-on-insulator trap

<table>
<thead>
<tr>
<th>Silicon</th>
<th>Silicon Dioxide</th>
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<td>30 μm</td>
<td>10 μm</td>
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A silicon-on-insulator (SOI) wafer with handle layer of 600 μm, SOI layer of 10 μm and a device layer of 600 μm. The silicon is doped withArsenic and has a resistivity of 0.001-0.005 Ωm. This process is similar to one used in J. Britton et al.¹

- A 40 nm layer of chromium is evaporated onto the surface followed by 500 nm of gold.
- The photoresist is spin coated on top of the gold and patterned.
- A deep reactive ion etch (DRIE) exposes the buried silicon dioxide.
- A 60 nm layer of chromium is evaporated onto the surface followed by 500 nm of gold.
- The gold then etched exposing the silicon.

Ion Trap Electrode Modelling

Electrode structures are drawn then using the Boundary Element Method (BEM) we can simulate electric fields between them. Using data taken from modelling the trap geometry it is possible to create the ponderomotive potential within the trap.

Simulations of a surface electrode geometry, these show potential contours corresponding to the trapping ponderomotive potential.

Calculating the position of the rf null towards the centre of the junction, below left, and evaluating the ponderomotive potential, the rf barrier and secular frequencies can be found, below right.

The solid line corresponds to the unoptimised rf geometry, a, the dashed line shows a reduction of approximately 6 μm with the modified geometry, b. This inset shows the rf null position towards the junction.

Above shows the radial secular frequencies from both a and b geometries. The secular frequency for the optimised geometry are shown in blue and red.

Cantilevered gold electrodes trap progress

Test samples have been included for both methods of fabrication to measure the voltage at which RF breakdown occurs. Two possible means of breakdown are suggested: bulk breakdown through the main body of the insulator and surface flashover, breakdown over the surface of the material. Samples were produce to test these breakdown mechanisms.

RF breakdown testing

Surface breakdown samples over quartz left and bulk breakdown through SOI-bottom.