Engineering of Microfabricated Ion Traps and Integration of Advanced On-Chip Features

Zak David Romaszko, Seokjun Hong, Martin Siegele, Reuben Kahan Puddy, Foni Raphaël Lebrun-Gallagher, Sebastian Weidt, Winfried Karl Hensinger*

Sussex Centre for Quantum Technologies, Department of Physics and Astronomy, University of Sussex, Brighton, BN1 9QH, United Kingdom

Abstract

Trapped atomic ions are a proven and powerful tool for the fundamental research of quantum physics. They have emerged in recent years as one of the most promising candidates for several practical technologies including quantum computers, quantum simulators, atomic clocks, mass spectrometers and quantum sensors. Advanced fabrication techniques, taken from established and nascent disciplines, are being deployed to create novel, reliable devices with a view to large scale integration and commercial compatibility. This review will cover the fundamentals of ion trapping before proceeding with a discussion of the design of ion traps for the aforementioned applications. We will analyse current microfabrication techniques that are being utilised, as well as various considerations which motivate the choice of materials and processes. Finally, we discuss current efforts to include advanced, on-chip features into next generation ion traps.

1. Introduction

The trapping of atomic ions within confining electric fields in vacuum was first conceived of, and demonstrated by, Wolfgang Paul and Hans Georg Dehmelt, securing them a share of the Nobel prize in 1989 [1], [2]. An ion isolated in this way can be extremely well decoupled from its environment and thus be cooled to record low temperatures using laser techniques such as those developed by David Wineland [3]. The extreme isolation and low thermal energy mean that the energy levels of the ion are highly stable and well resolved, with quantum states having been observed to remain coherent over several minutes [4]. This, along with the ability to prepare and detect the quantum states and generate high fidelity entanglement between trapped ions, make trapped ion systems a prime candidate for use in a wide range of fields that require the precise control of well-defined quantum systems. These include atomic clocks [5], quantum sensors [6], quantum simulators [7]–[9], mass spectrometers [10]–[12] and quantum computation [13], [14].

The Paul trap uses oscillating (RF) voltages to create a potential minima in up to three dimensions (see Figure 1.1), which, when combined with DC fields, is able to manipulate an ion's position [1]. With many of the applications of trapped ions comes the desire to significantly increase the number of ions while maintaining, and in some cases increasing, precise control over the position of individual ions. Quantum computing is a good example where many approaches to scalability require such a level of control [15]–[17]. This requires a significant reduction in the size and an increase in the number of control electrodes, making the early type of Paul traps, consisting of mechanically machined 3D electrode structures, unsuitable [18]. The use of microfabrication methods allows for the realisation of the required feature sizes, reproducibility and mass producibility needed for such devices. This led to several proposals in the early 2000's, with the first demonstrations of microfabricated ion traps seen in 2006 [19], [20], which were essential to demonstrate trapped ions as a viable candidate for the next generation of quantum technologies.

These 'trap-on-chip' devices utilise established fabrication techniques from the semiconductor and micro-electro-mechanical system (MEMS) industries to realise micron scale architectures in both 2D

*Z.Romaszko@sussex.ac.uk

(surface traps) [20], [21] and 3D configurations [19], [22]. Another set of well-established techniques, which is also highly prevalent in modern electronics, comes from complementary metal–oxide–semiconductor (CMOS) technology and has been used to successfully fabricate an ion trap [23].

In addition to the miniaturisation of the ion trap, the integration of peripheral components, such as photodetectors [24] and digital to analogue converters (DACs) [25], into the ion trap is also of great interest. Integration of these components allows the creation of compact devices and stand-alone trap modules and can also offer the potential to reduce electrical noise [26]. In addition, the integration of peripheral components may also be critical for large scale quantum computing with trapped ions where stand-alone modules are a key ingredient to scalability [16], [17].

To create an arbitrarily large quantum computer, the ability to connect between modules is required. Two methods that address the connectivity between modules have been proposed. One scheme, proposed by Monroe *et al.* [16], [27], uses photons, emitted by ions on separate modules, to initiate inter-module entanglement. Another method, proposed by Lekitsch *et al.* [17], relies on shaping electrodes in such a way that when neighbouring modules are closely aligned, ions can be transported from one module to another using electric fields.

This paper reviews the state-of-the-art of microfabricated ion traps including efforts to integrate advanced features such as optical components and electrical devices. In Section 2, the basic principles of ion trap electrode design are given. Conventional microfabrication techniques applied to ion traps are detailed in Section 3. Section 4 describes current research into integration of advanced features into an ion trap chip. Finally, Section 5 summarises this review with a discussion of the technological issues expected in the coming years. For further discussion of ion trap supporting hardware, and other ion trap fabrication reviews, we suggest refs. [28]–[33].

BOX 1: Evolution of ion trap structures

The first Paul trap (Figure 1.1(a)) used hyperbolic electrodes in a 3D configuration and was used for fundamental physics experiments [1]. This structure could only trap a limited number of ions, which limited the measurement accuracy of atomic resonances. To address this limitation, the linear Paul trap was developed [34], [35]. These traps consist of four machined rods assembled in parallel to confine ions radially and two end cap electrodes to axially confine ions [36], as shown in Figure 1.1(b). One of the most important characteristics of this linear trap is that ions in the same string share their motional modes. This feature gave rise to the first proposal of trapped ion based qubit operations by Cirac and Zoller [13].

The 4-rod trap can have high voltages (>1 kV) applied to it, which allows the creation of deep trapping potentials whilst maintaining stable parameters. The electrodes are also at a sufficiently large distance from the ions to minimise the effects of electrical noises from the electrodes. Segmenting these rods allows axial control of ions along a string. Owing to these strengths, 4-rod Paul traps are widely used in experiments performed on ion chains in situations that do not require microfabricated devices [37]–[40].

Notwithstanding the numerous successes of these ion traps, precise control is required for operations such as ion crystal separation, which could only be allowed by more electrodes of smaller sizes. To address this, lithographic techniques from the semiconductor industry were used to fabricate ion traps [19], [41]. These ion trap reproduced the 4-rod structure on a micron-scale, but the vertical distance between the electrodes was inevitably limited by the technical capability of thin film processes. As a solution that may offer advantages for general scalability, Seidelin *et al.* [20] proposed a direct projection of four rods onto a single plane resulting in a five-wire geometry which lays two radio-

frequency (RF) electrodes and three ground electrodes alternately, shown in Figure 1.1(c). This chip structure is referred to as a "surface electrode trap" (or "surface trap") and has become the most widely used geometry for microfabricated ion trap chips.
Advances in fabrication technologies have allowed more complex designs to be pursued [17],[22], [42]–[44].

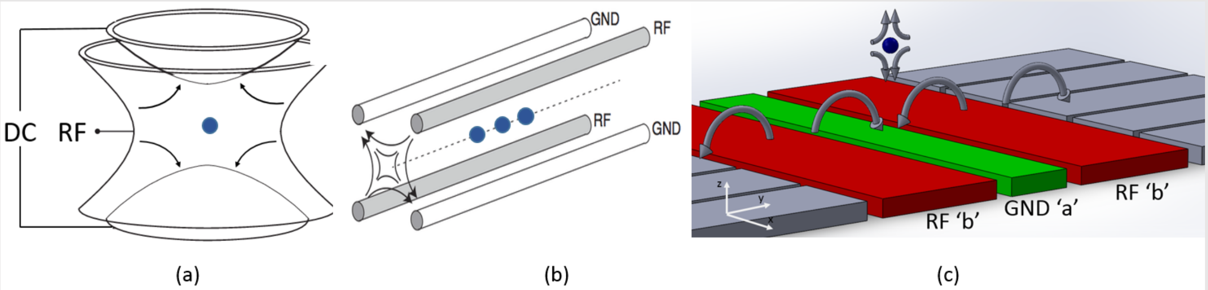

Figure 1.1. Evolution of electrode structure of ion traps with ions shown in dark blue. **(a)** The initial ion trap design which consists of a hyperbolic-structured RF electrode and two end-cap electrodes. **(b)** The linear trap with four linear rods assembled in parallel and two end-cap electrodes (not shown). **(c)** The surface ion trap chip in the conventional five-wire geometry where 'a' and 'b' represent the widths of the ground and RF electrodes respectively. In all figures, arrows indicate the direction of electric field when the RF voltage is positive.

Modern trap designs have, in part, been motivated by the creation of a trapped ion quantum computer. Concepts for trapped ion quantum computers were initially suggested by Wineland *et al.* [45] and Cirac *et al.* [46]. Following this, Kielpinski *et al.* [15] proposed an architecture in which ions are shuttled around a 2D array using time dependant electric fields generated by nearby electrodes. The array consists of regions that have specific functions, such as gate operations or ion storage, which are connected by linear and junction sections.

2. Ion Trap Geometries

This section will discuss basic ion trap geometries for top layer electrode design, as well as the geometrical considerations for ion transport and advanced ion trap designs. The basics of ion trapping are covered in Box 2.

2.1 Basic principles of five-wire geometry

Figure 2.1(a) shows a simplified planar view of a surface ion trap in a symmetric, five-wire geometry. An RF voltage is applied to a pair of linear electrodes while all the other electrodes are held at RF ground. The ponderomotive potential generated by the RF voltage confines ions parallel to the z axis at a height given by the widths of the RF and central ground electrode. Assuming infinitely long rails, the zero potential line from the RF, the RF nil, can be expanded along the longitudinal direction, and the axial position of the ions can be determined by static electric fields only. To generate the static electric field required for trapping or shuttling the ions in the axial direction, a calculated direct-current (DC) voltage set is applied to the segmented electrodes [47], [48].

The five-wire electrode geometry of surface ion traps has been analytically modelled in numerous studies [21], [49]–[51]. The width of the ground and RF five-wire geometry, 'a' and 'b' (as shown in Figure 2.1(a)) can be used to determine the trap depth, ψ_E, and ion height, h_{RFnil} [49];

Equation 1

$$\psi_E = \frac{e^2 V^2}{\pi^2 m \Omega^2} \frac{b^2}{(a+b)^2 + (a+b)\sqrt{2ab + a^2}},$$

Equation 2

$$h_{RFnil} = \frac{\sqrt{2ab + a^2}}{2},$$

where trap depth is the difference in the ponderomotive potential between the RF nil and the escape point, and Ω, e, m, and V indicate the trap frequency in Hz, elementary charge in Coulombs, ion mass in kilograms, and RF voltage amplitude in volts, respectively.

Generally, a deep trap depth, a high secular frequency, a low q-parameter, and a large ion height are preferred for stable ion trapping. Since these cannot all be achieved simultaneously (especially given differing scaling laws), a compromise should be determined by considering the constraints given by one's experimental setup [52], [53]. Nizamani *et al.* [53] analytically demonstrated that a ratio of RF and ground rails widths of b/a = 3.68, provided a maximised trap depth. However, this wide ratio, increases the distance between the outer DC electrodes and the trapped ions, thus reducing DC confinement. This balancing act is common place in ion trap design, and can depend heavily on purpose of the experiment and voltage range available on the electrodes. The longitudinal (axial) direction is not usually considered during simple, RF electrode design, since its properties are mainly determined by DC voltages.

2.2 Rotation of principle axes

In a typical experimental setup with a surface ion trap, laser paths are limited to the directions parallel or perpendicular (through a vertical hole penetrating the substrate [48]) to the surface of the trap chip. To be able to effectively Doppler cool in all 3 axes with only one cooling beam, the principal axes of the ion's motion must therefore be rotated (Figure 2.1). The rotation can be achieved by tilting the total electric potential at the ion position. The rotation angle can be calculated from the eigenvectors of the Hessian matrix of the total electric potential. To tilt the potential, there are two commonly used methods. The first approach uses RF rails of different widths, which rotates the pseudopotential [20], [50], [54]. The second method is achieved by applying asymmetric DC voltages to 'rotation' electrodes. As this will move the ion out of the RF nil, additional voltages are applied to control electrodes (Figure 2.1) and are required to compensate for non-zero fields [47], [55]. Asymmetric RF electrodes were initially used for surface traps, until proposals were made to rotate the principal axis using DC voltages on electrodes. The use of asymmetric DC voltages applied to these electrodes, became a popular approach since it could easily achieve a θ = 45° rotation angle [47].

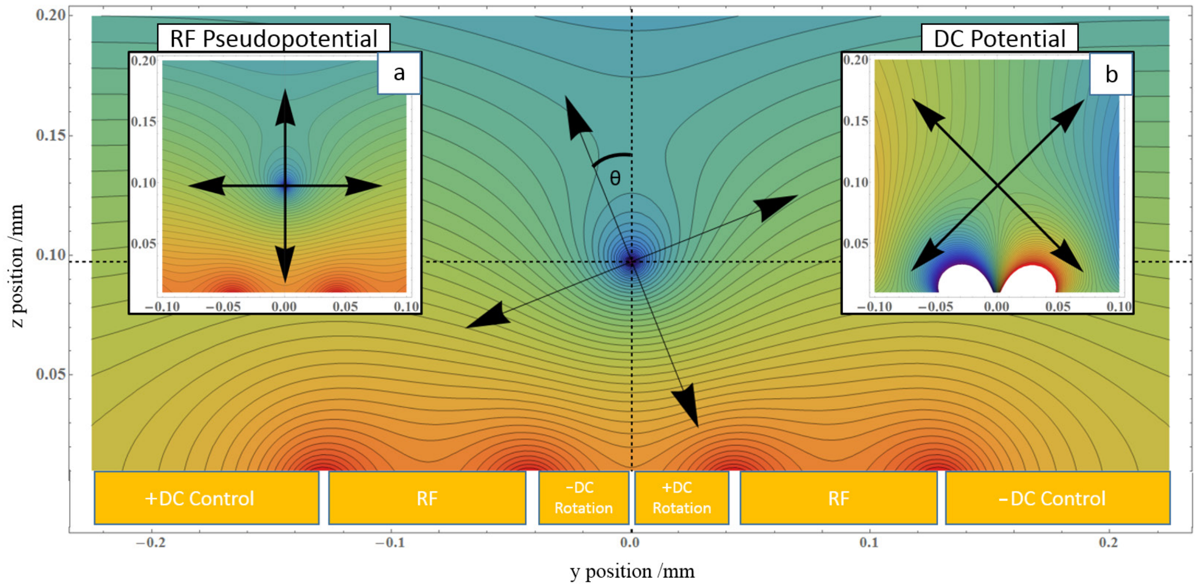

Figure 2.1. Method of rotating the principal axis by angle, θ using a 6 wire surface trap design [47]. The arrows show the principle axis in the radial directions. The central contour plot shows the total potential, φ_{tot} created from the superposition of **(a)** the RF Pseudopotential and **(b)** the DC rotation potential created by asymmetric voltages on DC electrodes.

2.4 Design and optimisation of geometries for ion transport

Some trapped ion uses, especially quantum computation, require the ability to move ions in a trapping potential such that certain operations are only felt on particular ions. Generally speaking, there are four types of operations required; linear shuttling, junction shuttling and separation and combination of ion pairs. These operations are carried out using time-dependent control electrodes which are located on the trap. The optimal geometries of these electrodes (in relation to electrode-ion distance) for operations such as linear shuttling and ion crystal (re)combination have been discussed in [49], [53]. These types of operations have been reliably shown with high fidelity [56]–[60], based on theoretical work in [61]–[63].

Having established the requirements for linear shuttling operations, we now move on to discuss the concept, complexities and requirements of designing and fabricating arrays of trapping zones arranged in a 2D plane first proposed in [15] and expanded towards and industrial blueprint for quantum computing in [17]. The first realisation of ion transport through a junction was demonstrated in a T-junction ion trap array [64]. Subsequent studies identified optimal geometries for ion trap arrays where linear regions are connected to others via junction nodes [65], [66]. At the centre of a junction node, three (T [64] or Y-junction [42]) or four (X-junction [67]) branches of linear rails join together, making the infinitely long rail assumption no longer valid. Consequentially, the uniform extension of the RF nil along the axial direction terminates at this point (Figure 2.2(a)). Changes in the ion's secular frequencies or moving over a pseudopotential barrier, such as that caused by a junction, can cause motional heating of the ion [67], [68]. To minimise these effects, geometry optimisation has been introduced to improve junctions [66], [69], [70]. Most of the optimised geometries are created using iterative optimisation methods such as a genetic algorithm. Using these designs, a number of successful experimental results of junction transport have been reported [42], [67], [71], achieving fidelities as high as 99.8% for 10^6 transports, e.g. ion transport fidelity well below the relevant fault-tolerant threshold [69].

Whilst the previous designs are used for generic ion traps, for quantum simulations, two-dimensional ion lattices of stationary ions (with small inter-site distances) can be beneficial and ion traps to create these lattices have been successfully fabricated as a mechanical structures [52], and subsequently as a microfabricated ion trap chip [43]. Schmied *et al.* [72] present a useful tool for creating geometries required for close lattice sites. Using this tool, lattice geometries have been fabricated with close, inter-site distance and multiple degrees of freedom per site [44]. This tool has also been used to investigate bi-layer ion traps [73].

2.5 Numerical Simulation Tools

For complicated geometries, such as junctions and loading slots, analytical methods are no longer viable, therefore numerical simulations of electric fields are essential for designing electrodes. In the early years of surface traps, the boundary element method (BEM) was used to simulate simple geometries with a single electrode layer [74], owing to the available computational resources. Advances in computational power have meant that the finite element method (FEM) has become a viable simulation tool and geometries with greater complexity, including structures for oscillating magnetic field gradient schemes (see Section 4.1), are routinely modelled and optimised using this method [70], [75], [76].

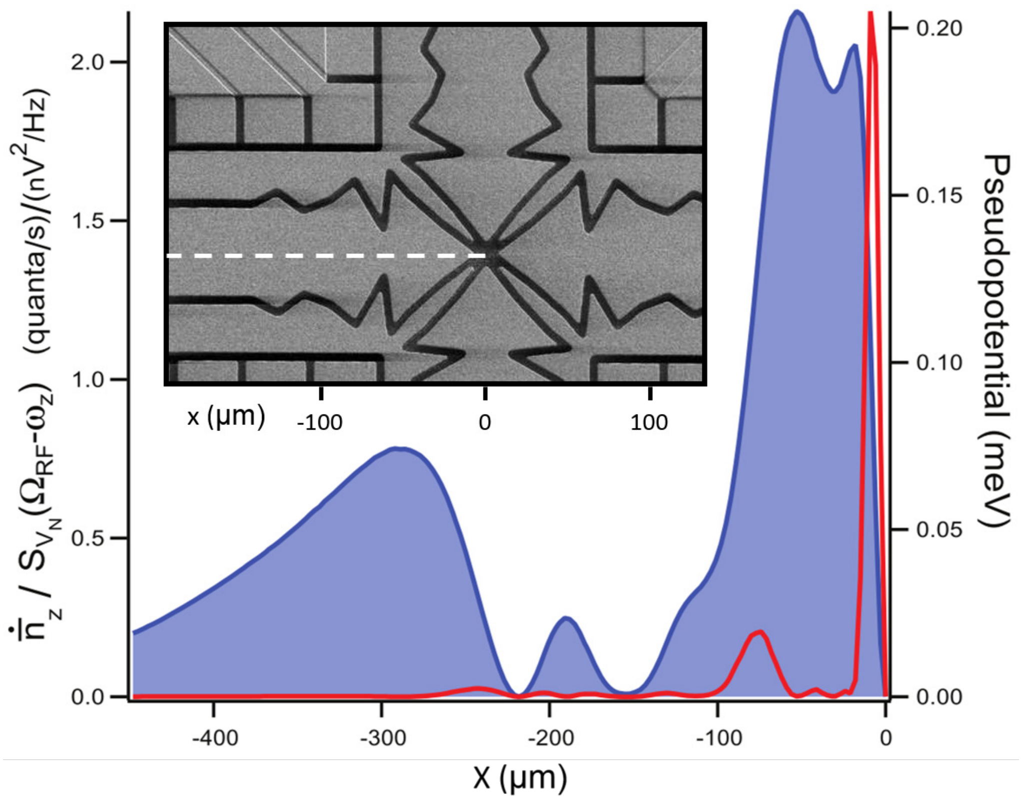

Figure 2.2. Optimised x-junction electrode geometry at the junction centre to reduce the distortion of the RF pseudopotential (blue shaded) at the ion height and motional heating (red line), normalised by the spectral voltage noise, S_{V_N}. The trap potential is evaluated for a ^{40}Ca ion with V= 91 V_{rms} and Ω= 2π x 58.55 MHz. Figure taken from [69] and modified for continuity.

BOX 2: Ion trapping 101

A simplified in-vacuum setup of a typical, microfabricated, surface ion trap experiment is shown by Figure 2.3.

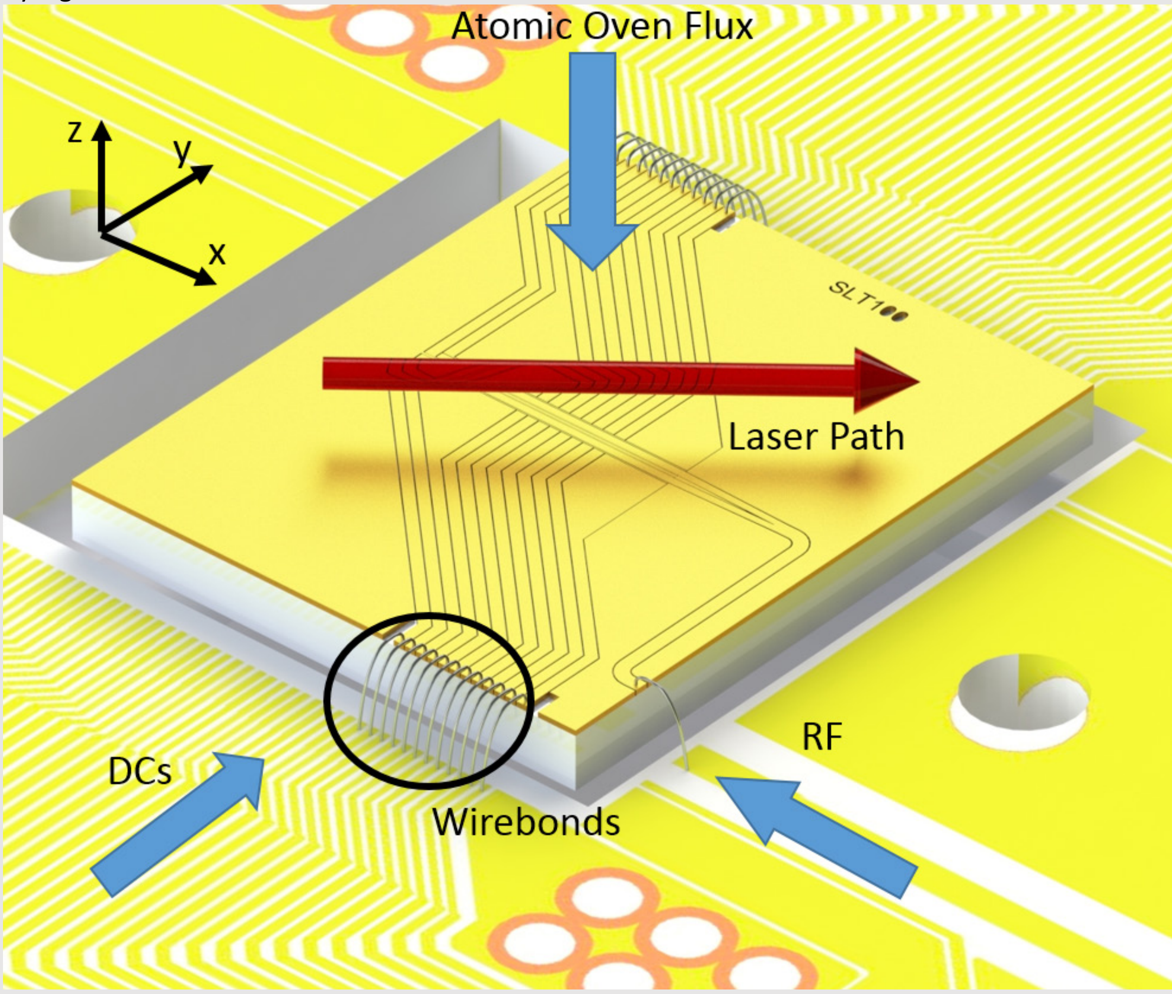

Figure 2.3 – A typical ion trap experiment setup. Ions are trapped in an ultra-high vacuum chamber with feedthroughs to connect the ion trap to supporting electronics and viewports for optical access.

By applying an RF voltage to the ion trap, one is able to create a trapping potential. Quasi-static DC fields (sometimes time dependant) are applied to electrodes and are used to confine the ion in the axial direction [1]. This can be expressed as,

Equation 3

$$\varphi_{tot}(x,y,z,t) = \varphi_{DC}(x,y,z) + \varphi_{RF}(x,y,z)\cos(\Omega t)\,,$$

where φ_{tot}, φ_{DC} and φ_{RF} is the total, DC and RF potential respectively and Ω is the frequency at which RF is being driven.

The equations of motion for a particle in a Paul trap are given by

Equation 4

$$\ddot{x} + \frac{e}{mr_0^2}(\varphi_{DC} - \varphi_{RF}\cos(\Omega t))x = 0\,.$$

These equations follow that of the Mathieu equations which have the form

Equation 5

$$\frac{d^2 i}{d\zeta^2} + (a_i - 2q_i\cos(2\zeta))i = 0\,.$$

Whilst there are an infinite number of solutions to the Mathieu equations, only a small subset of these solutions are stable which are given by the Floquet theorem [77].
The ions motion can now be characterised in two ways, 'secular motion' and 'micromotion'. The secular motion is the motion due to the curvature of the electric field potential. This is an important feature required to implement spin-motion coupling [78]. Micromotion is an often unwanted part of the ion's motion [36]. Micromotion arises when the ion is not in a zero potential of the RF (otherwise known as 'RF nil') and hence subject to an additional, oscillatory component of motion. When creating electrostatic wells to confine an ion, it is important to make sure both the DC and RF nil are at the wanted ion position to reduce micromotion. The secular motion of an ion describes the motion from being a particle in a potential well. The secular motion of an ion is discussed in more detail in Leibfried *et al.* [79].
An atomic oven with a small aperture creates a flux of atoms parallel to the trap surface [80] during which process a laser is used to ionise the atoms [81]. The atomic flux can also lead to unwanted surface coating, and many efforts have been made to reduce this and are discussed in Section 3.
To initially cool the ion, Doppler cooling is employed [82]. When Doppler cooling, all 3 directions of motion must be considered to effectively cool the ion. To cool the in-plane directions of motion, the laser is typically positioned at a 45° angle with respects to the planar motion, to have cooling components acting in both 'x' and 'y' motion. The 'z' motion can be effectively cooled by rotating the principal axis using the methods discussed in Section 2.2. Additional lasers and laser paths may be required to perform laser based quantum logic operations [83].
The final consideration for ion trapping is optical access to the ion. Wirebonds are often used to connect the trap to a supporting printed circuit board (PCB). If the wirebonds are in the path of a laser, unwanted scattering will occur, which will drastically affect the ability to perform experiments. To image the ion, external optics, combined with charged-coupled devices (CCDs) and photo-multiplier tubes (PMTs) are employed. These sensors and optics are typically outside the vacuum system however efforts are being made to integrate the required technology for the detection of ions into the ion trap structure (see Section 4.2).

3. Ion Trap Microfabrication Techniques

This section covers material considerations as well as the fabrication processes required for surface ion trap chips.

The semiconductor industry revolutionised the creation of miniature, electronic devices using patterned conducting and insulating materials, with the most common example being CMOS. Key to this success are highly reliable and reproducible processes using well established fabrication facilities (foundries). Microfabricated ion traps have been created which use these foundries [23], [25]. However, as will be outlined in Section 3.1, some ion trap specific requirements which necessitate structures which do not use established processes (such as formation and subsequent patterning of thick dielectric layers) or materials (such as gold and copper) which are not permitted inside many foundries. As a result, modern ion trap fabrication borrows many techniques from across microfabrication, such as MEMS, with the eventual goal of achieving reproducible processes such as those used in CMOS.

3.1 General considerations for the microfabrication of ion trap chips

Critical features which should be addressed when designing ion trap chip structures and the required fabrication processes are as follows.

1. The electrodes should be able to sustain a RF voltage suitable for that ion species (heavier ions require larger voltages). A higher RF voltage allows trapping of ions farther from the chip surface, reducing the effects of the electrical field noise and laser scattering from the chip surface. In addition, higher voltages can allow for higher trap depths and secular frequencies.
2. Coupling of the RF field into the substrate should be minimised to prevent power loss and heating of the device [65].
3. The area of dielectric exposed to the trapped ions should be minimised. In general any dielectric should be sufficiently shielded such that electric fields from trapped charges on the dielectric, are not felt by the ion. This is because factors such as ultraviolet (UV) lasers incident on dielectric surfaces can generate time-varying, stray charges in the dielectric [84]–[86], which in turn cause unwanted, time-dependent, ion displacements.
4. All the materials, including various deposited films, should be compatible with ultra-high vacuum (UHV) environments. The chip should also be able to withstand processes required to achieve UHV such as baking and cryogenic temperatures.
5. There must be clear optical access between lasers sources, detectors and the ions. This for example, requires that wirebonds do not impede the optical path.
6. Exposed surfaces should be contaminant free and surface roughness minimised to the greatest extent to reduce anomalous heating of ions [87]–[89] and unwanted laser scattering.

3.2 Substrate materials

This review describes a typical fabrication process for ion traps using a silicon substrate. Apart from substrate shielding methods, microfabrication processes remain broadly similar for all substrates.

Designing a fabrication process for ion trap chips starts with the selection of layer materials, since the number and dimensions of thin film layers can drastically change the complexity of the whole process. Dielectric and conductive (or semi-conductive) substrates have their own distinct advantages and disadvantages. Use of dielectric substrates allows for a very simple fabrication process as well as low power loss and heat in the substrate. However, accurate bulk micromachining of dielectric substrates for introducing vertical penetration holes and buried metal layers can be difficult. Another concern is that of exposed dielectric surfaces between electrodes causing stray fields [84].

Silicon, the most widely used material in modern semiconductor technology, has the advantage of utilising most processes that are not compatible with insulating substrates. It is, however, very lossy in the mid-range resistivity (10^2-10^4 Ω cm) for RF frequencies [90]. To compensate this, the simplest and most widely used method is to place an additional metal layer referred to as a 'ground plane' (M1) between the RF electrode and the substrate. Although this adds complexities to the fabrication of silicon ion trap chips, as detailed in the next subsection, it is widely adopted since it almost guarantees the successful shielding of the substrate from RF dissipation. Another approach is to use very high or very low resistive substrates [91]. In this case, the temperature dependence of the silicon resistivity should be considered - at cryogenic temperatures, silicon can even act as an insulator [92].

3.3 Standard fabrication processes for ion traps

Figure 3.1 shows a typical fabrication process of a silicon based ion trap chip, which consists of a ground layer (M1), an electrode layer (M2), and two dielectric layers (D1 and D2) that are used to electrically isolate the conducting layers and the substrate. The process starts with the deposition of a dielectric layer on the silicon substrate, which insulates the ground plane from the substrate. A 1-2μm layer of either SiO_2 or SiN_x is used for this, and is typically grown using plasma enhanced chemical vapour deposition (PECVD) or as a thermal oxide. A ground plane, M1, is deposited on the D1 layer (Figure 3.1(a)) using any UHV compatible conductive material such as Au, Al, Cu, etc. This is commonly a 1-2μm layer, either sputtered or evaporated onto the device. When developing chips with vertical interconnect access (VIAs) to improve electrode routing, these thin insulating and conducting layers can be stacked multiple times [93]. Since high RF voltages applied between the electrodes and ground plane are desirable in surface ion traps, the D2 layer separating the two metal layers should therefore be thick, so as to maximise the voltage at which electrical breakdown occurs. Thus, the thickness of the D2 layer is generally on the order of 10 μm, with the deposition and etching of this layer usually being the most difficult steps throughout the entire ion trap fabrication (Figure 3.1(b)). This is because such vertical dimensions are generally not covered by conventional semiconductor processes, which also limits the material choice for the dielectric layer to PECVD SiO_2 or SiN_x. Bautista-Salvador *et al.* [94] demonstrated a polymer-based, spin-on dielectric for ion trap fabrication, which allowed for thick dielectric layers. Deposition and patterning of the top metal layer (M2) can be performed by using conventional microfabrication processes including electroplating, sputtering, evaporation, and plasma dry-etching (Figures 3.1(c), (d)). Since the top layer is directly exposed to the trapped ions, more factors should be considered when selecting the electrode material. Gold is one of the widely used materials for the top metal layer owing to its extremely low oxidisation rate. However, since gold is not compatible with many conventional microfabrication techniques, it is also possible to deposit a thin gold layer on the aluminium electrodes afterwards [95]. The final step etches the dielectric layer in both vertical and lateral directions to reduce the effect of charges trapped on the dielectric surface. The vertical etching of the thick dielectric layer (Figure 3.1(e)) uses the electrode pattern as a mask, and reactive ion etch (RIE) to etch. This is followed by isotropic wet or gas etching of the dielectric sidewalls (Figure 3.1(f)), which helps to minimise the exposure of the ions to trapped charges [55].

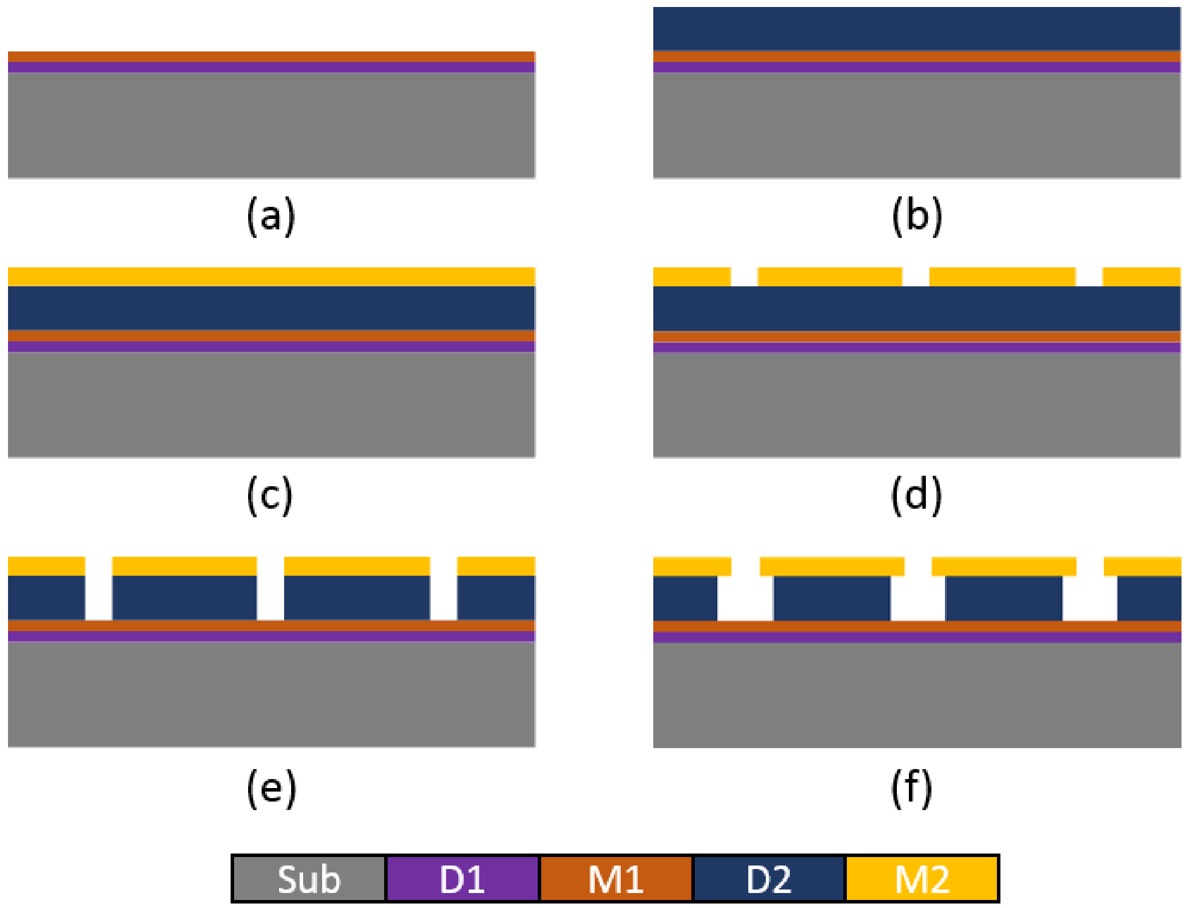

Figure 3.1. A conventional fabrication process flow of a surface ion trap chip. **(a)** Forming a ground plane and an insulating layer that isolates the ground plane and the substrate. **(b)** Deposition of a thick (~µm's) dielectric layer. **(c)** Forming a metal layer on the dielectric. **(d)** Etching of the metal layer to define the electrode patterns. **(e)** Subsequent etching of the thick dielectric layer. **(f)** Isotropic etching of the dielectric pillars from the sidewalls to reduce the area of dielectric sidewalls exposed to the ion.

Additional fabrication processes for a vertical slot penetrating the silicon substrate can also be included as part of the ion trap fabrication, using a conventional deep silicon etching process. This hole is used to load neutral atoms from the backside of ion trap chips to reduce the atomic flux onto the chip surface [96]. Also, the hole can be used as an optical path for increased laser access or for the detection of fluorescence from the ion [97]. Eltony *et al.* [98] used a transparent material, indium tin oxide (ITO), as the electrode layer to allow for the detection of fluorescence emitted from ions with a photodetector underneath the electrode on the backside of the trap chip.

The fabrication methods described here address common processes required to implement a silicon-based ion trap chip. Microfabricated ion traps can also be fabricated by many alternative processes not discussed in this review [28], [31], [94], [99]. Furthermore, fabrication processes have been optimised for specific capabilities, such as extremely high breakdown voltage [43], [100] or entire shielding of dielectric sidewalls [86]. Finally, when considering the integration of advanced features, processes can become more complicated, which will be discussed in greater detail in Section 4.

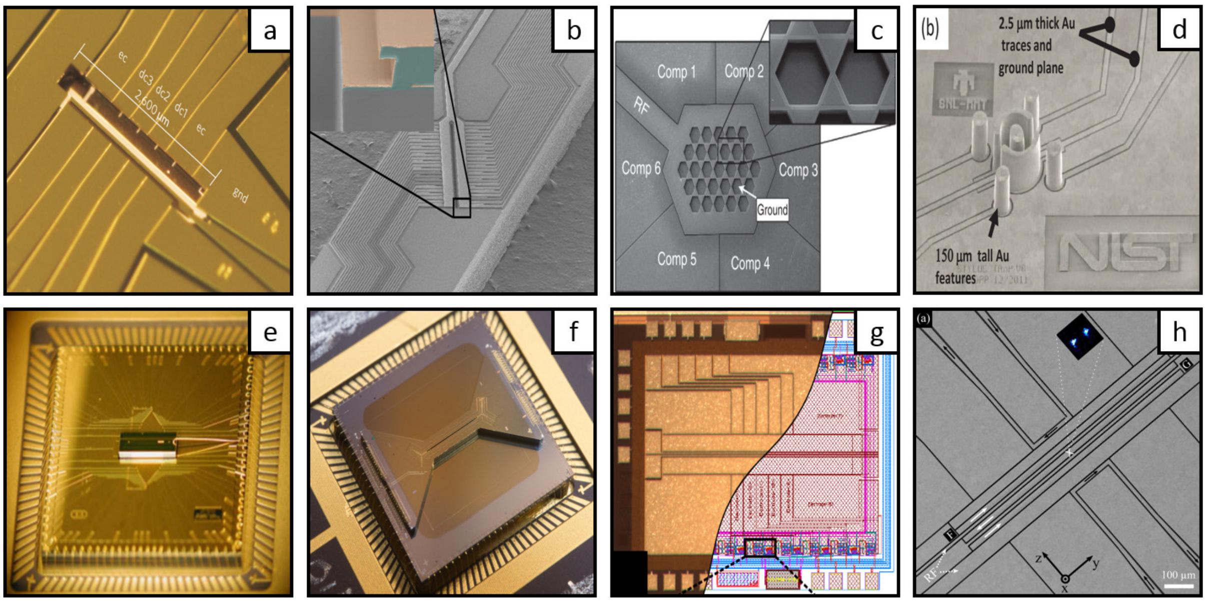

Figure 3.2 – Images of reported ion traps **(a)** Microfabricated, 3D quadrupole trap **-** National Physics Laboratory (NPL) - Wilpers *et al.* [22] **(b)** Low dielectric exposure - Seoul National University – Hong *et al.* [86] **(c)** First 2-D array on a chip and high breakdown voltage - University of Sussex – Sterling *et al.* [43] **(d)** Large metal structures – National Institute of Standards and Technology (NIST) – Arrington *et al.* [101] **(e)** Through Silicon Via (TSV) in an ion trap - GTRI/Honeywell – Guise *et al.* [93] **(f)** High optical access – Sandia National Laboratory (SNL) – Moehring *et al.*/ Maunz [42], [48] **(g)** Ion trap fabricated in a CMOS foundry - Massachusetts Institute of Technology (MIT) – Stuart *et al.* [25] **(h)** Novel fabrication method for thick metal/dielectric layers - Physikalisch-Technische Bundesanstalt (PTB) – Bautista-Salvador *et al.* [94].

BOX 3: Efforts to deal with heating rates

Despite many successful implementations of surface traps, miniaturising the ion trap structure has also created a number of side effects, and one of the drawbacks is the so-called "anomalous heating" of trapped ions [102]. This is thought to be induced by electric field noise from the surface of trap electrodes. The electric field noise can couple to the ion motion when the frequency is near the motional frequency of the ion, which in turn leads to the increase of phonon number and gate error. Many efforts have been made to investigate this both theoretically [103], [104] and experimentally [105]–[107]. One method of reducing the heating rate is by increasing the distance, d, between the ions and the electrode surface, since it has been experimentally shown that the heating rate scales as ~d^{-4} [106], [108], [109]. However, given that the maximum voltage that can be applied to a trap chip is limited by current semiconductor technologies, an increased distance inevitably leads to a shallower trap depth, therefore there is a limit to how much d can be increased by. Another method to reduce the heating rate is by cooling the ion trap to cryogenic temperature, first demonstrated in [106]. A number of publications showed that this approach can reduce the heating rate by two orders of magnitude [54], [106], [110]. Another approach is in-situ cleaning of the chip surface [87], [111]. Since hydrocarbon-based contaminants adsorbed on the electrode surface during the bake-out process are suspected to be a major source of the electrical noise, inducing anomalous heating [112], removal of the contaminants after the bake-out can also reduce the heating rate by two orders of magnitude. Owing to these efforts, extremely low heating rates of ions have been reported [91]. More work is required and is currently under way to better understand the source of anomalous heating [113]–[115].

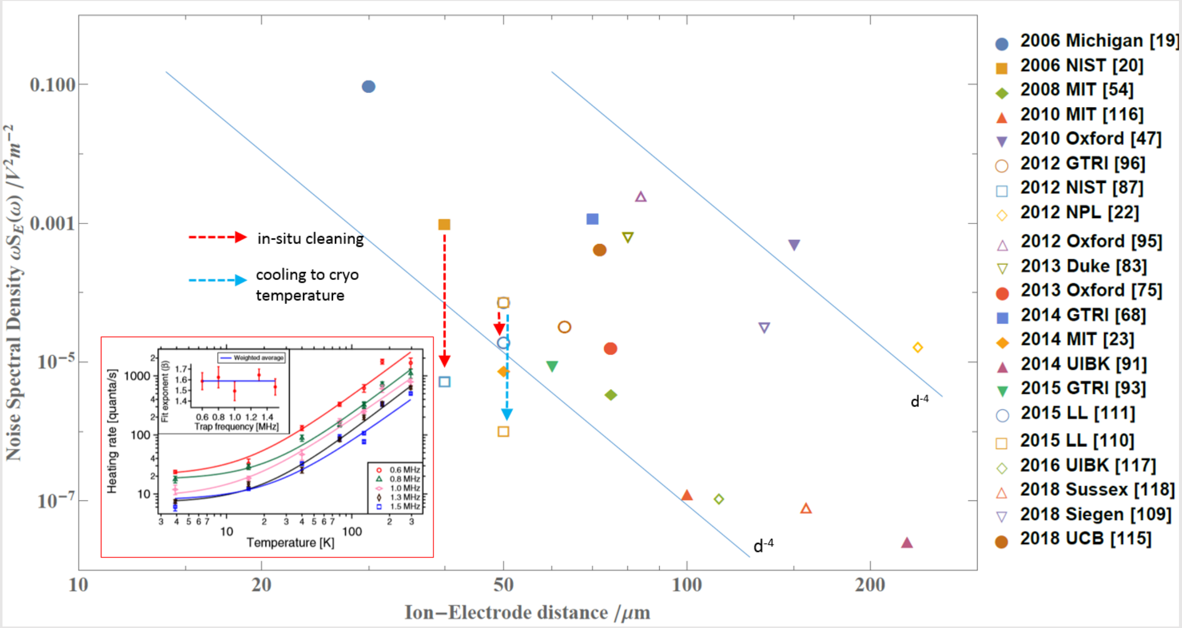

Figure 3.2. Measurement results of heating rates on surface ion traps from different research groups. The heating rates measured in a cryogenic environment (blue-dotted circle) are noticeably lower than that of room temperature systems. The red and blue arrows indicate the changes made in the same experimental setup by in-situ surface cleaning and cryogenic cooling, respectively. The inset (taken from Bruzewicz *et al.* [110]) shows the temperature dependency on heating rate, showing significant gains from room temperature to cryogenic temperatures.

4. Advanced On-Chip Features

As ion trap geometries become more complex, either for quantum simulation or scalable computation purposes, supporting systems are often required to sit within the footprint of the ion trap device [17]. Such efforts include integrating optical and electrical devices used in experiments into the microchip. These approaches can also contribute to the miniaturisation of precise measurement units such as atomic clocks and mass spectrometers, combined with efforts to miniaturise vacuum chambers [27], [119].

This section will mainly discuss research into chip-level integration of advanced features.

4.1 Embedded Gate Schemes

Several schemes for quantum logic gates between qubits rely on magnetic field gradients, either static [120], [121] or oscillating [122], [123]. Three methods to create the gradient have been used: permanent magnets, placed near the trap to produce a static gradient at the ion position [121], [124]–[126]; in-plane current carrying wires (CCWs), fabricated as part of the electrode layer, which allow the creation of both static and oscillating magnetic field gradients [75], [127]–[129]; sub-surface current carrying wires (CCWs), fabricated below the electrode and ground plane layers [130].

Permanent magnets are commonly implemented to realise the static gradient scheme, achieving gradients of up to 36 T m^{-1} [126]. Scaling up to large systems may prove difficult due to careful, manual alignment of the ion trap to the magnets begin required.

In-plane CCWs have been shown to provide oscillating gradients of up to 54.8 T m^{-1} [76]. In this scheme the trap geometry must be altered in order to accommodate the CCWs and the power dissipation must be considered. The power dissipation could be reduced by using thicker layers, to decrease resistance, but in most designs this is set by the lithographical methods used for the electrode layer, typically less than 5 µm.

Sub-surface CCWs, situated beneath the ion trap, do not impinge on the electrode design but can only be used for static gradients due to shielding by induced currents in the ion trap electrode and ground plane layers. The device of Welzel *et al.* [130], used Cu wires 127 µm thick, fixed to an AlN chip carrier and mounted 285 µm below the trap surface. A gradient of 16 T m^{-1} was achieved using a current of 8.4 A.

Larger gradients could be achieved with sub-surface CCWs by reducing the wire to ion distance. Lekitsch *et al.* [17] suggest that the CCWs could be imbedded into the substrate surface, using the dual damascene process, and the ion trap fabricated directly above the wires. By embedding the CCWs into the substrate not only is the trap to wire distance decreased but thermal sinking is improved, thus greater current, and therefore higher gradients, should be feasible [17]. Researchers at the University of Sussex have already demonstrated applying a current of 11 A (corresponding to a current density of 10^6 A cm^{-2} to an ion microchip which should result in a magnetic field gradient of >185 T m^{-1} at an ion height of 125 µm. At an ion height of 40 µm, this method is expected to produce a gradient in excess of 1,000 T m^{-1} or conversely obtain ~185 T m^{-1} with significantly lower current required (~3A).

Whilst a relatively new technology for ion traps, CCWs are common place in the atom-trapping community, where large, steep magnetic fields are used to trap neutral systems [131]–[134]. The currents and wire dimensions used for atom trapping are similar to those required by trapped ion gate schemes and therefore much of what has been learned in the atom trapping field may also be applicable.

4.2 Optical Components

For many trapped ion technologies addressing and state readout of ions is required using optical techniques on an individual ion basis. It is sometimes beneficial that such optical components are integrated in the device, to increase the fidelity of addressing and readout operations. This subsection will look at several integrated optical components and examine their uses.

Optical fibres have many uses in trapped ion experiments for both addressing and readout operations. The typical structure of a fibre however does not naturally suit itself to an ion trapping experiment as an exposed dielectric near the ion can significantly disturb the trapping field. By integrating an optical access hole, the dielectric can be shielded by the ion trap itself, allowing for fibres to be brought close to the ion [97], [135], [136].

To address multiple ions, integrating waveguides into the ion trap is a promising way forward. Mehta *et al.* [137], [138] demonstrated a multi-ion addressing technique with integrated silicon nitride waveguides and grating couplers to address individual ions, with a total optical system loss of 33dB. Using this, a single qubit gate was performed with 99% fidelity.

Integrating mirrors into the ion trap surface can allow for more photons from the ion to be collected, by reflecting otherwise lost photons. Merrill *et al.* [139] integrated micro mirrors into their surface ion trap, enhancing photon collection by 90% which resulted in a collection efficiency of 14% (numerical aperture of 0.69). Ghadmi *et al.* [140] showed a 4.1(6) % coupling of the fluorescence from a 174Yb+ ion into a single mode fibre using integrated diffractive mirrors, which nearly tripled the bulk optics efficiency. Integrated mirrors can also be used to create cavities on chip to, for instance, facilitate atom-light coupling for photonic interconnects. Towards this endeavour, ion traps fabricated on top of high-finesse optical mirrors to create a cavity have been demonstrated [141], [142]. There remains, however, some development before strong coupling, already demonstrated macroscopically [143], can be achieved in such a microfabricated device.

Integrating photodetectors into the ion trap can be beneficial as it can significantly reduce the ion-detector distance. This, as a result, increases the number of photons which reach the detector, allowing for increased fidelity or faster measurements. Kielpinski *et al.* [144] and Lekitsch *et al.* [17] suggested using integrated single photon avalanche diodes (SPADs) for light detection. Eltony *et al.* [98] presented a transparent trap made of ITO with an integrated photodetector featuring a collection efficiency approaching 50%. Slichter *et al.* [24] showed UV-sensitive superconducting nanowire single photon detectors (SNSPD) made of MoSi, integrated into a microfabricated ion trap. This device demonstrated 76(4)% system detection efficiency at a wavelength of 315nm with a background count rate below 1 count per second. The trapping field decreased the system detection efficiency by 9%, but did not increase background count rates. Being a superconducting device however, the stringent requirement on the operating temperature (3.2K) introduces additional challenges, depending on the application. The use of SPADs however only requires temperatures of 70K in order to achieve a performance of that similar to a photo-multiplier tube [17].

4.3 Passive Components

Capacitors, resistors and inductors are a key part of any ion trapping experiment for use in filtering, resonators and general electronics [95], [119], [145], [146]. Bringing these devices on-chip can have a multitude of benefits, from increased density to reduced noise via closer proximity to the device.

One method of high-density integration of passive components takes advantage of advanced CMOS facilities by integrating a CMOS die. Guise *et al.* [26] first showed this by integrating a Semiconwell

SWTF[1] 12 channel, bare-die RC filter array (35kΩ, 220pF) on to a PCB. To attach the die, a standard low-outgassing silver epoxy was used, and channels were connected using wirebonds. Whilst not integrated on chip, the attach methods are similar to that used by industry on silicon dies, hence could be integrated on an ion trap if required.

Another option is to fabricate a capacitor into the trap with two metal planes separated by a dielectric. Trench capacitors take advantage of increased surface area by etching vertically into silicon using well established processes. This allows for a substantial increase in the capacitance per unit area. For ion traps, this was first demonstrated by Allcock *et al.* [95], who integrated trench capacitors into their trap, which allowed 1nF to be achieved in a 100μm square. This was 30 times higher than the capacitance allowed in the same area when using a conventional, planar, fabrication process.

To create the low-noise, high voltage RF trapping field, a helical resonator is commonly employed [147], [148]. At the heart of the design is the ability to impedance match using inductors. Efforts have been made to reduce the bulky nature of the device to a more manageable size [149], [150], but have yet to be integrated into a device. Microfabricated inductors [151] could be one route forward in this respect. For future devices, microfabricated inductors could also be used to replace the standard low-pass filter [95] with more advanced filters, such as a band-stop filter, to remove noise on DC electrodes.

4.4 Active Components

Rent's Rule [152] suggests that computers were only successful by changing the scaling law on the number of inputs required to control bits. The same thinking has also been suggested for quantum computation [153]. These connectivity problems naturally lead to the introduction of active components into the vacuum system [26], or even into the ion trap [25]. One of the key requirements for ion-trapping is that all integrated components must be UHV compatible [154]. This often eliminates the use of packaged electronics, making bare-die the alternative for inclusion in a UHV environment. Packaged components can sometimes be permitted if also operating at cryogenic temperatures. Guise *et al.* [26] introduced two, 40 channel DACs (AD5370) into an UHV environment. For this experiment, the AD5370 was not sourced in bare-die form, but instead a standard, packaged, AD5370 was used and then decapsulated using nitric and sulphuric acid [155]. Assembly is as discussed in Section 4.3. Whilst this is a novel method to overcome low supply of bare-die products, it is likely that future devices using this method would already be in bare-die form, hence suitable for ultra-high vacuum.

Stuart *et al.* [25] recently integrated a custom, CMOS DAC into an ion trap design. The custom DAC was designed for the CMHV7SF 180nm node from Global Foundries. Key to this node is the ability to allow for higher voltages (20V span) compared to typical <5V span, thus allowing the implementation of an amplifier for voltages more suited for ion trapping. A switching device was also included to disconnect the ion trap from the DAC when not updating, hence reducing noise when disconnected. As the electrode acts as a capacitor with low leakage current, the switch can disconnects the DAC whilst the electrode holds a voltage. The ion trap on top was also fabricated as part of the CMOS process, similar to that used by Mehta *et al.* [23]. A common concern with semiconductor devices is 'freeze-out' at low temperatures, where the energy required to overcome a band-gap is insurmountable. However the device previously mentioned was operated at cryogenic (4K) temperatures and more complicated devices such as a field programmable gate array (FPGA) have also been shown to work at such temperatures [156].

[1] http://www.semiconwell.com/rc_net/swtf.htm

4.5 Stacked Wafer Technology

It has been proposed that back-side connections to the ion trap will be required for large-scale quantum computers to connect to its supporting systems [93]. Lekitsch *et al.* [17] expand this to use wafer stacking of different components of the quantum computing stack, such as DACs, detectors, and cooling. These proposals require the introduction of through-substrate-via technology, often known as through-silicon-vias (TSV). The first demonstration of these technologies in ion traps was reported by Guise *et al.* [93], who connected to an ion trap via a backside ball-grid array and TSVs. In [93], the ion trap die is attached via a ball-bonding method, which uses a programmed gold ball bonder to leave individual short, gold studs on an interposer. A localised eutectic bond is then used to connect the interposer to the back-side of the device. Due to the size of devices, a wafer-scale system can have issues with high stress, reducing connection quality [157]. On a wafer-scale, the studs are commonly microfabricated as opposed to using a ball bonder [158]. Eutectic bonding is also not the only option for wafer-scale attaches and many other, commonly used, methods exist [159], [160].

Lekitsch *et al.* [17] suggest the implementation of micro-channel cooling as part of the stacked wafer proposal. This could also be used in other architectures, either for power dissipation or to reduce heating rates. Whilst they have yet to be introduced into ion traps, micro-channel coolers have started to emerge for room temperature devices capable of removing >300W/cm^2 [161]. Riddle and Bernhardt [162] demonstrated a micro-channel cooler using liquid nitrogen capable of removing 1000W/cm^2, considerably helped by an order-of-magnitude increase in thermal conductivity of Silicon at ~70K [163]. Difficulties with this design however may emerge from heat-flow between stacked wafer levels.

5. Conclusion

Much progress has been made in recent years on the development of complex microfabricated ion trap. Whilst the creation of custom potentials through simulations is well understood, many questions still must be answered in terms of the integration of advanced technologies. We present Figure 5.1 as a summary of the requirements for many different advanced ion traps. With most of these technologies having already been individually demonstrated in trapped ion experiments, the microfabricated ion trap is expected to form a fundamental component of quantum technologies.

5.1 Outlook

Demand for quantum technologies, as a commercial product, requires that devices can be made on a large scale, with high reliability and yields. The following section will discuss the current state of these industries with respect to previously discussed technologies.

Many of the proposed technologies discussed will require CMOS devices integrated into the ion trap. However, unlike the standard operation environment of CMOS, ion traps are often required to work at cryogenic temperatures. Interestingly, cryogenic control electronics is also a priority for superconducting qubit platforms [164]. Cryogenic CMOS integration of a DAC has recently been demonstrated by Stuart *et al.* [25] . By being a CMOS process, this has already shown that the capability by industry is there to integrate a DAC. Separate from the ion trapping community, a more complex device, an FPGA, has been shown to work in a cryogenic environment [156]. Whilst commercialised SNSPDs are relatively uncommon, SPADs are becoming increasingly wide-spread, with high demand from the driverless car market. SNSPDs may prove simpler to integrate as they can be fabricated as part of the ion trap, however, they have to be operated at superconducting temperatures. Wafer stacking and TSVs, whilst nascent technologies, are becoming prevalent in many different modern devices, such as high-bandwidth memory [165], and is a well-understood process [166]. However, in these industries, low yields are acceptable. Cooling requirements will become increasingly important to consider when integrating different technologies. Microchannel coolers provide a promising path towards managing the potential future thermal requirements however, they have yet to reach market.

Whilst fabrication and assembly industries allow individual aspects of an ion trap to be demonstrated, combining these expertise will be essential for creating a more advanced ion trap.

5.2 Concluding Remarks

In this paper we have motivated modern design choices in ion traps and highlighted their relevance to modern experiments. We have covered the basics of ion trapping and how ion traps fit into a typical experiment. We discussed how ion trap geometries are determined and how they are adapted to novel designs for different applications. We presented a typical fabrication flow for a modern device by looking at current state-of-the-art fabrications, as well as efforts to tackle heating rates. We examined advanced on-chip features such as optical components, electronics, and methods to integrate this into modular structures. Finally, we highlighted what the authors believe to be the current struggles in microfabricated ion traps and how these conform to modern industrial capabilities.

Trapped ions constitute an extremely powerful system to realise and control quantum phenomena such as entanglement and superposition showcasing unmatched fidelities and coherence times. The emergence of ion microchips allows us to incorporate the advantages of modern microfabrication and microprocessor advances to this system giving rise to a fully scalable hardware platform for a wide range of quantum technologies.

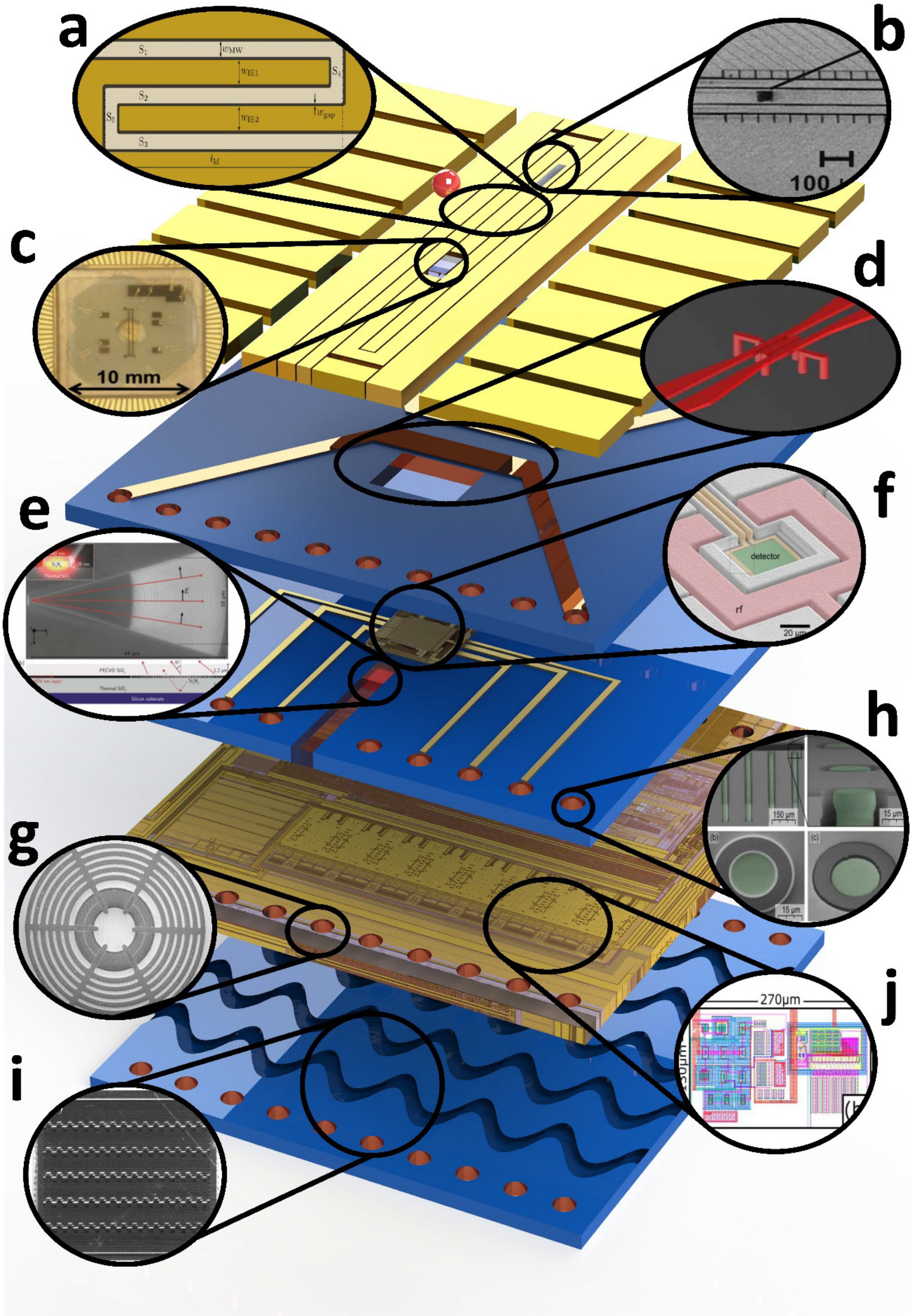

Figure 5.1 – Advanced on chip technology in an ion trap. It should be noted that not all features are required and their necessity is dependent upon use case. **(a)** Oscillating gradient CCWs [128] **(b)** Backside loading [69] **(c)** Transparent ITO electrode [98] **(d)** Static gradient CCWs [17] **(e)** Si_3N_4 grating for individual optical addressing [138] **(f)** Integrated photon detector [24] **(g)** Trench capacitors [69] **(h)** Through Silicon Vias (TSVs) [93] **(i)** Integrated electronics [25] **(j)** Microchannel cooling [161].

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