Development of monolithic 3D ion traps microfabricated using SiO_2-on-Si

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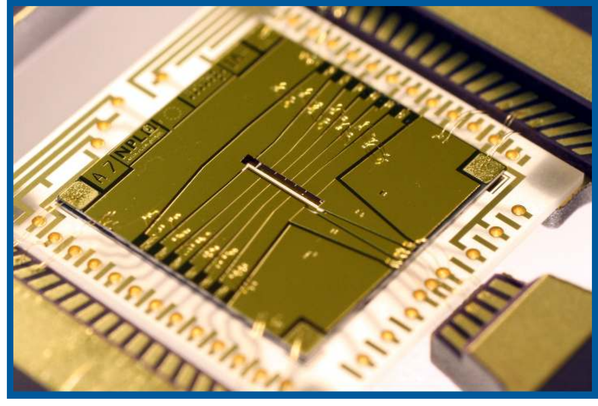


Motivation

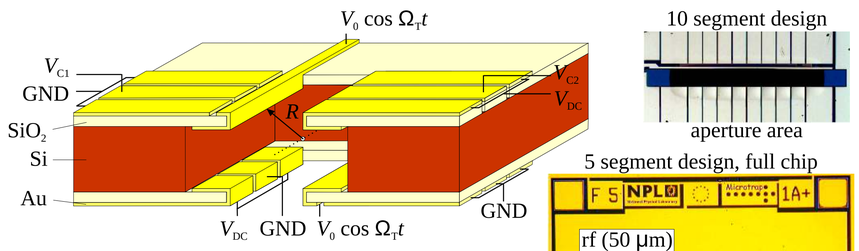
Microfabricated traps are a necessary component to achieve scalability for ion trap QIP. Previous successful traps have included 1) 2D surface traps [1,2], 2) 3D Au coated alumina [3-5],3) 3D degenerate Silicon [6], 4) monolithic 3D GaAs traps [7].

We have developed a design for a microfabricated ion trap based on SiO_2-on-Si technology [8] for use in optical clock and QIP applications. The trap potential and electrical operating characteristics have been modeled, the fabrication process developed and fully processed traps are now available. The design offers

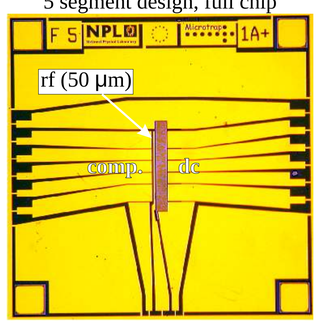
* manufacture based on planar processing to create a 3D trap,
* a monolithic design: no post-processing assembly,
* scalability to many segments,
* a unit aspect ratio: high efficiency, deep potential and
* low RF heating.

Present limitations on mechanical integrity and RF voltage amplitude have been addressed and solution are to be implemented shortly. Loading trials in a first trap are taking place at present.

Concept

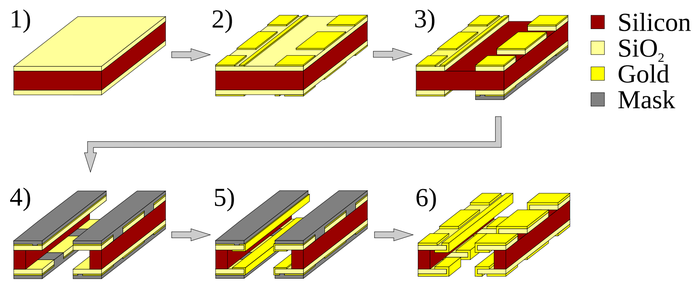


5 segment design, full chip



Si Thickness	500 → 150 µm
Ion-electrode distance, *R*	350 → 90 µm
SiO_2 Thickness	15 µm
Au Thickness	5 µm
Au Surface roughness	< 50 nm RMS
Undercut	300 → 250 µm
Si Resistivity	10^{-3} Ωcm

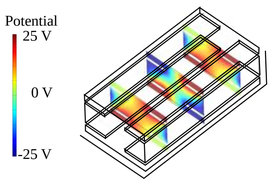
Fabrication method



1) Thermal oxidation (15 µm) of a highly doped silicon wafer.
2) Evaporate Au electrode pattern.
3) Anisotropic ICP etch of SiO_2 to create DC-fingers and aperture.
4) Isotropic DRI etch through Si to give trapping region.
5) Shadow evaporate Au into undercut.
6) Electroplating to 5 µm thickness of Au.

Modelling

Finite element modelling of trap in 2D and 3D to calculate static potentials due to RF and DC electrodes.



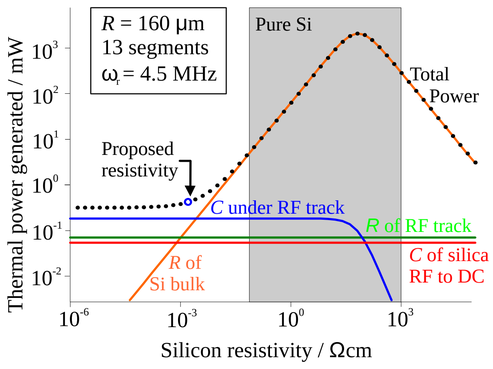
Then calculate [9] resultant pseudopotential for $^{88}Sr^+$ using MATLAB.

Typical operating parameters
assuming trapping of $^{88}Sr^+$.

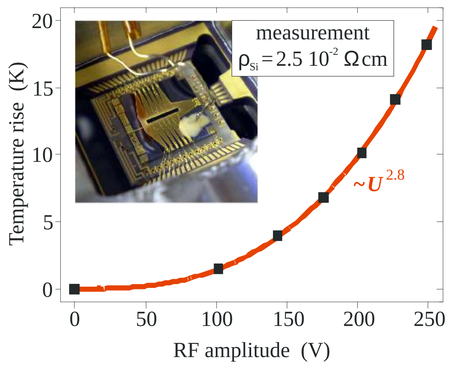
Parameter				**Unit**
R	160	90	30	µm
V_0	170	54	5.5	V
V_{DC}	5.1	1.6	0.18	V
RF Freq., $\Omega_T/2\pi$	21	21	21	MHz
$\omega_r / 2\pi$	4.5	4.5	4.5	MHz
$\omega_z / 2\pi$	2.0	2.0	2.0	MHz
Radial depth	5	1.5	0.15	eV
Trap efficiency	70	75	79	%

RF dissipation and heat generation

Highly doped bulk silicon



Low resistive heating



Measurement results

* Heat is well conducted and spread through Si bulk.
* CLCC package transports heat to airside.
* Worst case estimate: 0.4 mW heat generated results in a 10 K temperature rise.
* Decreased trap size leads to lower RF voltages and reduced power dissipation.

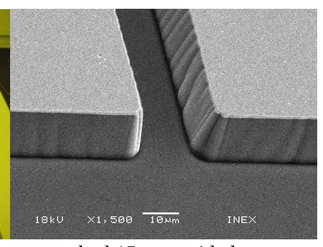
Ohmic contacts to silicon

* Contact resistance < 0.1 Ω, fully ohmic
* ensures bulk silicon is grounded

Planar SiO_2-on-Si technology

Processing is based on a monolithic, parallel technology used in photonics industry.

patterned 4” wafer

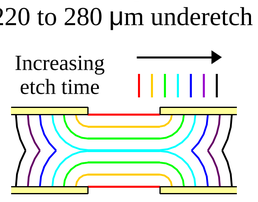


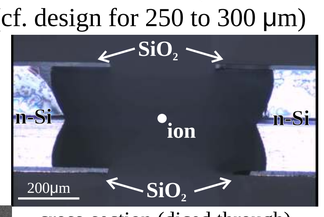
etched 15 µm oxide layer

basis: highly doped n-Si wafer, 2.5 10^{-3} Ωcm
Si-MAT, Germany: 15 µm of thermal oxide
INEX, Newcastle: patterning, 15µm oxide etch, double sided processing

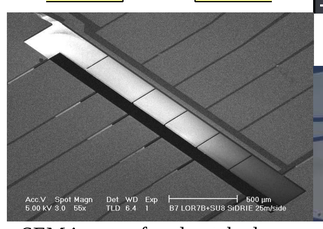
Underetch

* 2-sided isotropic DRIE for underetch of n-Si (in-house)
* 220 to 280 µm underetch (cf. design for 250 to 300 µm)

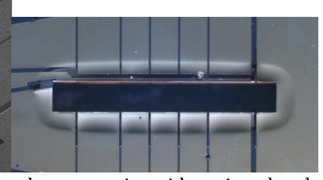




cross-section (diced through)



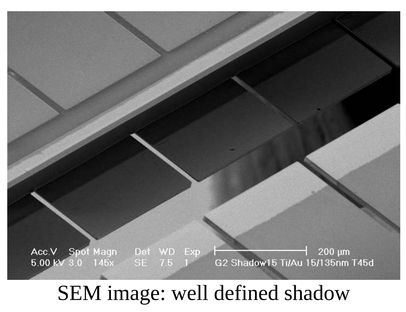
SEM image of underetched area



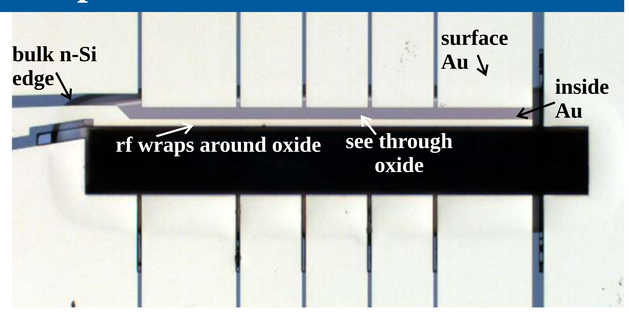
shear stress in oxide: ~ 1µm bend

Shadow evaporation

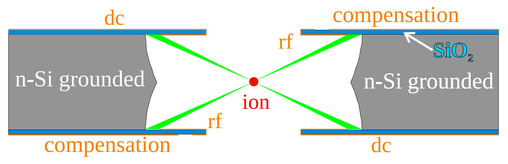
In-house development of shadow evaporation for metallisation of electrodes’ internal surfaces.



SEM image: well defined shadow



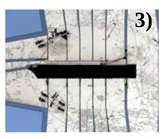
Evaporation to within 50 µm of n-Si allows one to
* minimise the solid angle of dielectrics seen from ion,
* maximise the ion’s direct view of electrodes.

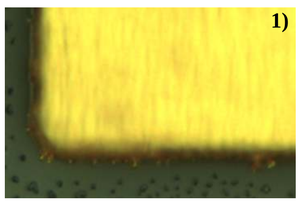


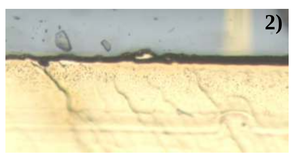
Electroplating of the 3D structure

Initial problems:
1) dendritic gowths on micron level
2) uneven inside coverage
3) dirty plating

Introduced:
* oxygen plasma ash cleaning
* Metalor ECF64 pure Au plating
* tight temperature and pH-control
* stepwise plating of in- and outside electrodes with direct line of sight of bias field lines

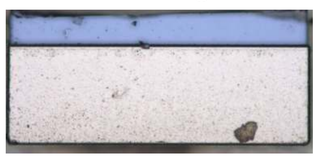




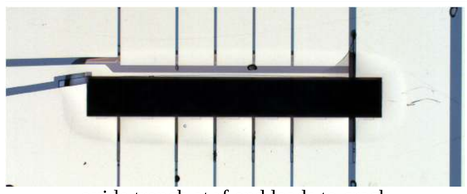


Achieved:
* smooth surfaces and edges, Ra < 50 nm

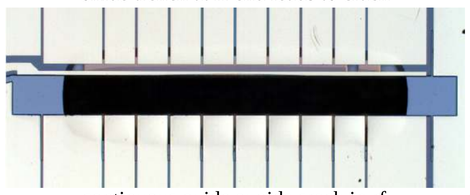
* homogenous internal coverage



Structural integrity



oxide trench at rf end leads to crack



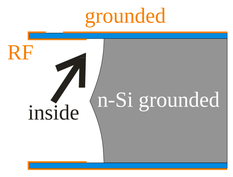
continuous oxide avoids crack in rf

Electrode breakage generally is low. An asymmetry of shear stress at RF electrode end appears to lead to cracking. Avoiding this asymmetry eliminates fractures.

“Cantilevers” resonate ~ 200 kHz, fracture > 30 kV rf.

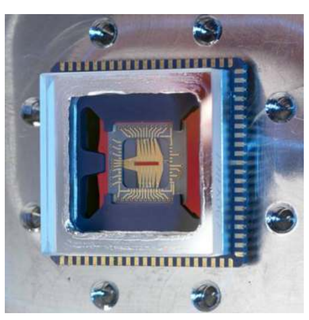
Electrical breakdown

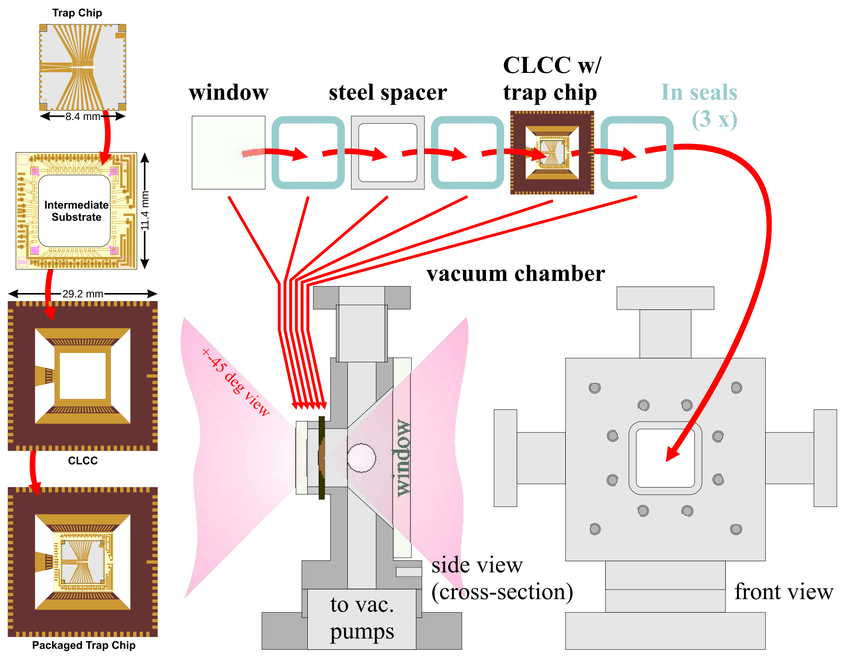
* Likely due to *surface flashover* between DC and RF electrodes at above ~ 400 V/µm [10].
* Our design keeps field < 5 V/µm; DC-tests up to 12V/µm show no problems.
* RF-tests: flashover occurs on inside of most tested chips at ~1V/µm assumed to be due to Au scattered during shadow evaporation onto inside insulator surface; SIMS shows Au there.
* Etching 50 nm of oxide after plating increases breakdown threshold.

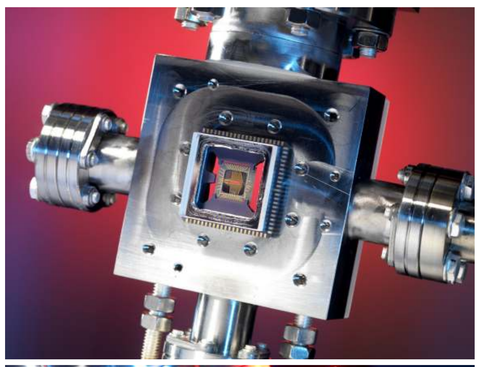


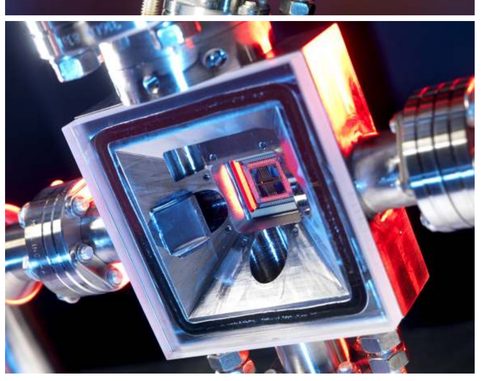
Electronic & vacuum package

Advantages
* mutiple electrical feedthroughs
* UHV compatible ~ 3 10^{-11} mbar
* excellent optical access
* compact design
* fast turn around
* no in-vacuum electronics
* potential for further miniaturisation









Conclusions&Outlook

We have designed and fabricated a linear RF ion trap to the constraints of a microfabrication process using gold-coated silica-on-silicon that is based on planar processing techniques used in the photonics industry.
* 3D unit-aspect ratio affords deep traps with high efficiencies,
* Au electrodes,
* highly conductive grounded silicon spacing layer,
* RF heating does not limit the trap performance,
* monolithic design,
* no post-processing assembly of electrodes,
* scalable to many-segment geometries.

We are now aiming to demonstrate the performance of our monolithic, microfabricated, 3D, unit aspect-ratio linear ion trap for QIP.

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