Microfabricated ion traps for quantum information and simulation

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Introduction

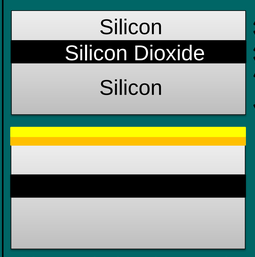
The design and implementation of scalable ion trap fabrication methods is of key importance for ion trap quantum computing. A scalable ion trap quantum computer will require hundreds to thousands of control electrodes. Building such traps using conventional machining and assembly is a daunting if not impossible task and only realistic if microfabrication can be successfully harnessed to construct microfabricated ion trap arrays. This will allow large trap arrays to be produced without manual assembly and with higher levels of precision.

Currently several challenges face the implementation of microfabricated ion traps:

- Exposed dielectrics (uncontrollable static fields)
- Limited rf voltage (reduce trap depth and secular frequencies)
- Large ion heating rates.
- Geometries may not allow adiabatic transport
- Ability to scale

Here we show are work towards overcoming these challenges.

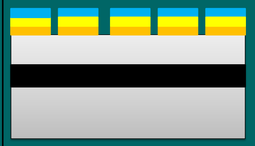
Silicon-on-insulator trap



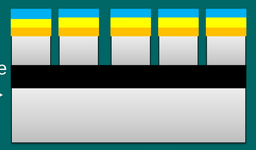
A silicon-on-insulator (SOI) wafer with handle layer of 600μm, SiO_2 layer of 10μm and a device layer of 30μm. The silicon is doped with arsenic and has a resistivity of 0.001-0.005 Ωcm. This process is similar to one used in J. Britton et al[1].

• A 40nm layer of chrome is evaporated onto the surface followed by 500nm of gold.

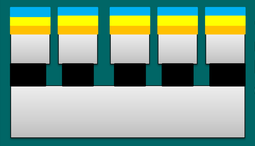
• Photoresist is spin coated on top of the gold and patterned



• The gold then chrome are etched exposing the silicon.

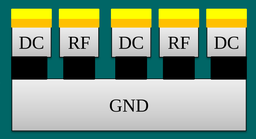


• A deep reactive ion etch (DRIE) exposes the buried silicon dioxide.



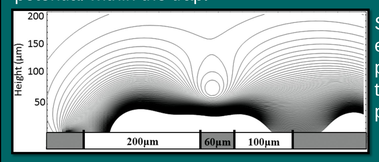
• An isotropic hydrofluoric acid (HF) etch removes the silicon dioxide and undercuts beneath the silicon hiding all exposed dielectrics from the ion.

• The photoresist is removed with acetone leaving the final trap geometry.



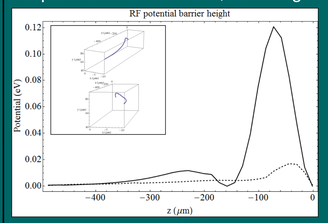
Ion Trap Electrode Modelling

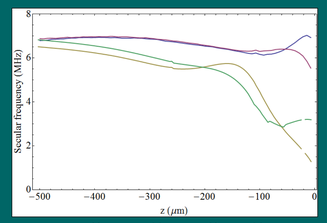
Electrode structures are drawn then using the Boundary Element Method (BEM) we can simulate electric fields between them. Using data taken from modelling the trap geometries it is possible to create the ponderomotive potential within the trap.



Simulations of a surface electrode geometry, these show potential contours corresponding to the trapping ponderomotive potential.

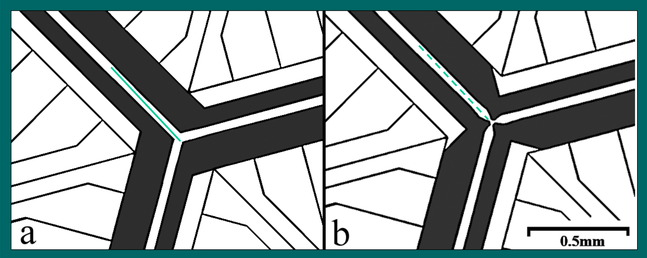
Calculating the position of the rf nil towards the centre of the junction, *below left*, and evaluating the ponderomotive potential, the rf barrier and secular frequencies can be found, *below right*.

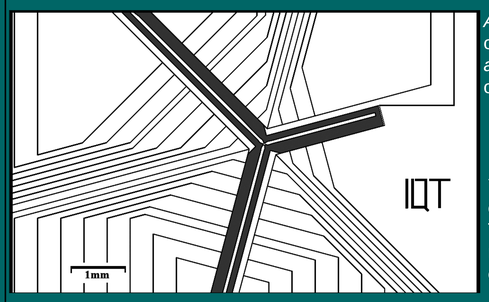




The solid line corresponds to the unoptimised rf geometry, ***a***, the dashed line shows a reduction of approximately 6 with the modified geometry, ***b***. The inset shows the rf nil position towards the junction.

Above shows the radial secular frequencies from both ***a*** and ***b*** geometries. The secular frequency for the optimised geometry are shown in blue and red.

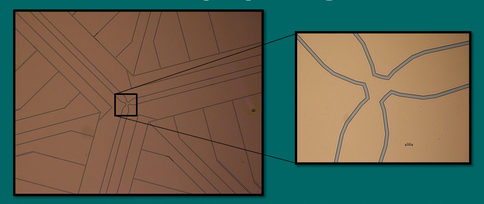




Above left shows original geometry, *above right* shows optimised geometry.

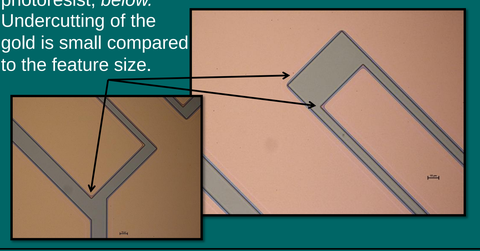
Y junction with 44 control electrodes. The dark grey represents the RF electrode.

SOI trap progress

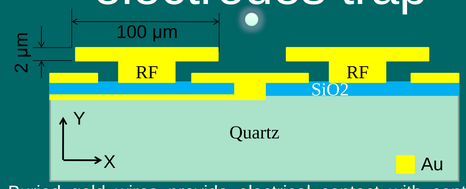


Chrome and gold deposition and etch have been achieved *above* with some small undercut of the gold beneath the photoresist, *below.*

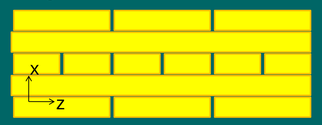
Undercutting of the gold is small compared to the feature size.

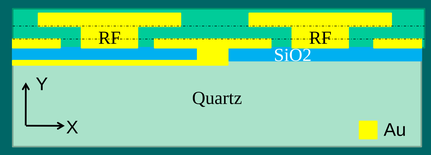


Cantilevered gold electrodes trap



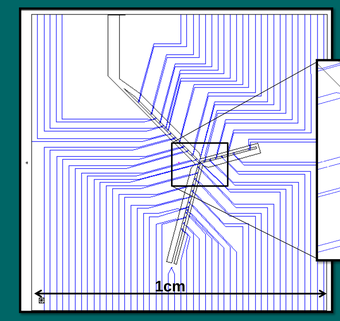
Buried gold wires provide electrical contact with central control electrodes. This provides better ion control with lower DC voltages.



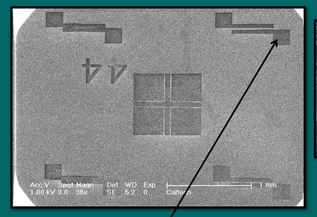


Dashed lines correspond to photoresist (green) layers, after each layer is deposited and developed gold is electroplated, by repeating this a cantilevered structure can be achieved.

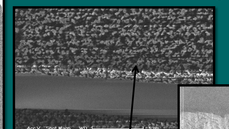
Cantilevered gold electrodes trap progress



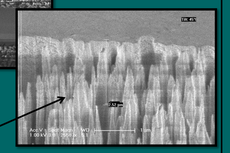
Buried electrodes mask, the buried wire layout that will be etched into the quartz substrate before being filled with gold.



Deep reactive ion etch

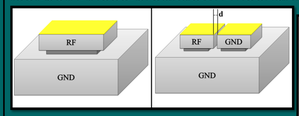


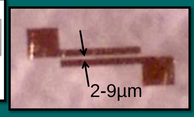
DRIE leaves quartz pillars



RF breakdown testing

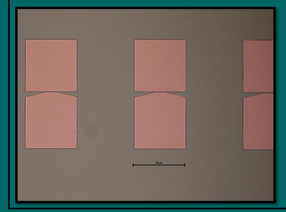
Test samples have been included for both methods of fabrication to measure the voltage at which RF breakdown occurs. Two possible means of breakdown are suspected: bulk breakdown through the main body of the insulator and surface flashover; breakdown over the surface of the material. Samples were produce to test both these breakdown mechanisms.

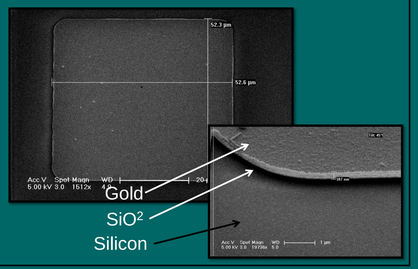




Surface breakdown samples over quartz *left* and bulk breakdown through SiO^2 *bottom*

SOI bulk test *left* and closely spaced electrodes *right & bottom.*





1) J. Britton, D. Leibfried, J. A. Beall, R. B. Blakestad, J. H. Wesenberg and D. J. Wineland, *App Phys lett*, 95, 173102 (2009)