Towards Cryogenic Surface Ion Traps

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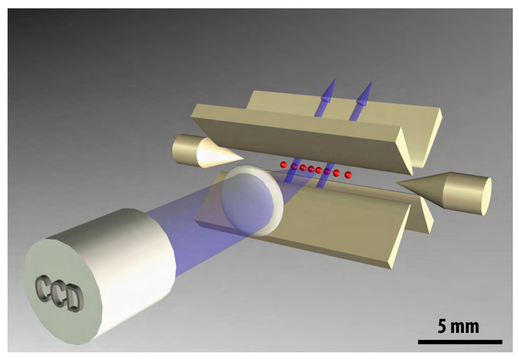
Motivation

Scalability to many ions remains one of the most significant challenges for ion trap quantum computing.

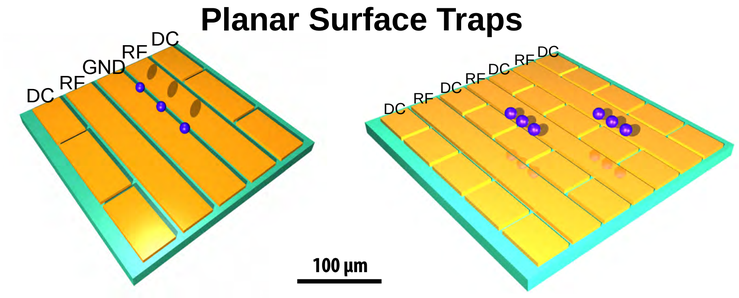
Micro Ion Traps

Traditional Ion Traps



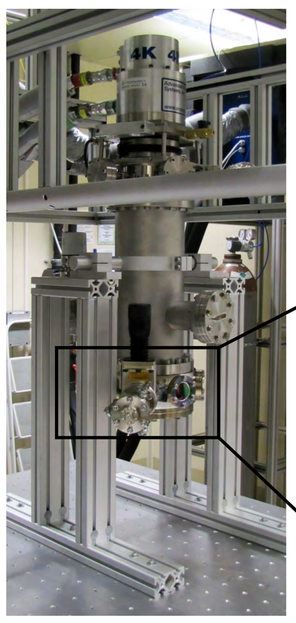
example of a macroscopic linear Paul trap

Planar Surface Traps

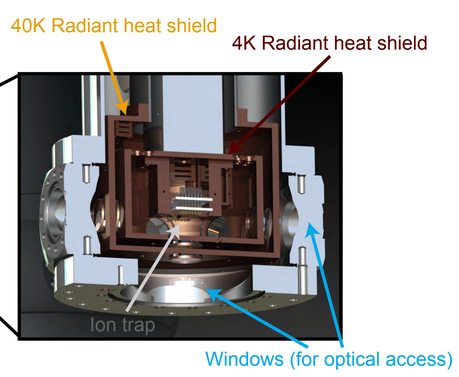


- Electrodes in single plane
- Ions trapped above that plane
- simple fabrication
- segemented traps allow shuttlling between different processing zones

Cryogenic System: Gifford McMahon Cooler



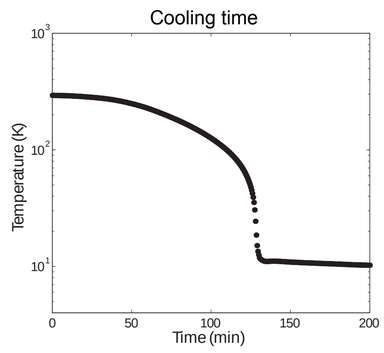
Ion-heating rate can be reduced by ~2 orders of magnitude by cooling trap from 300 K to 6 K[1]

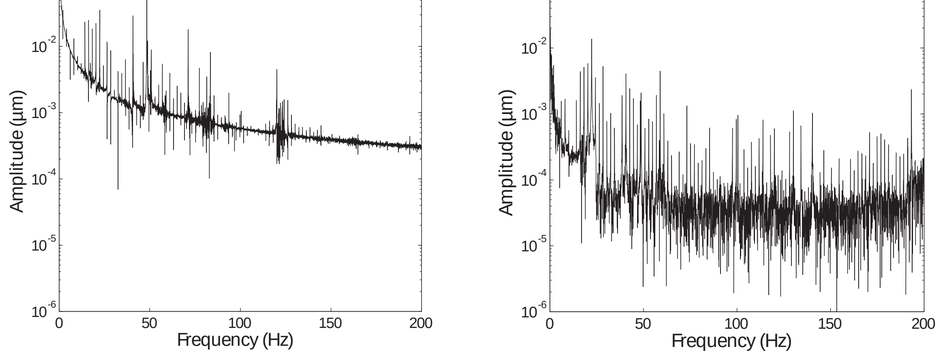


[1]J. Labaziewicz et al., Phys. Rev.Lett. **101**,180602 (2008)

Setup

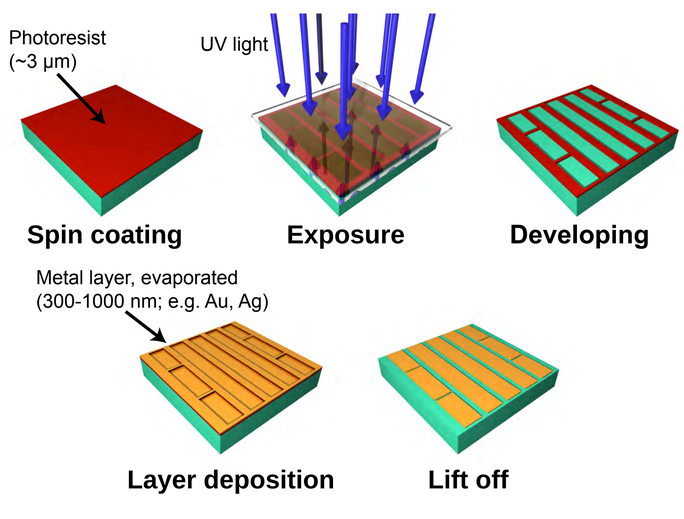
- Sample temperature ~6-10 K
- Easily implemented UHV conditions
- Good optical access
- Fast trap-testing turn-around times (few days)
- Low vibrations: vibration isolation interface
  no mechanical coupling between cryocooler and vacuum chamber





Trap Fabrication by Photolithography

Lift-Off Process

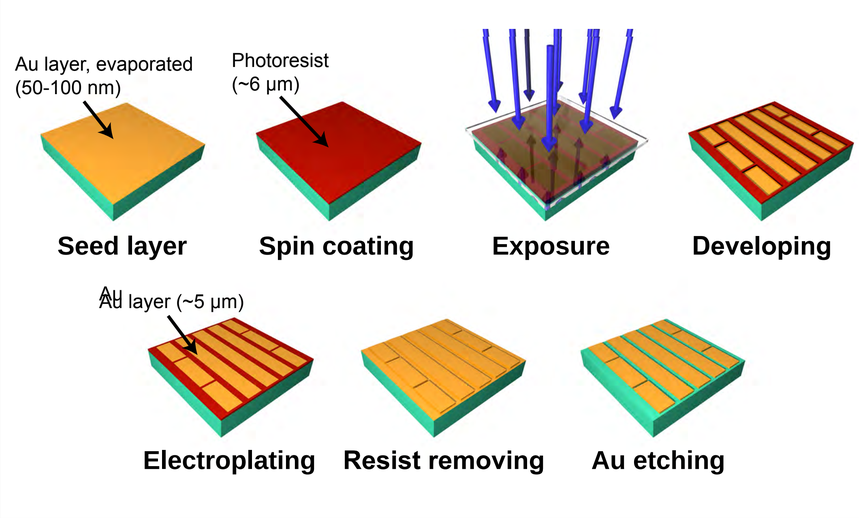


Lift-Off vs. Electroplating

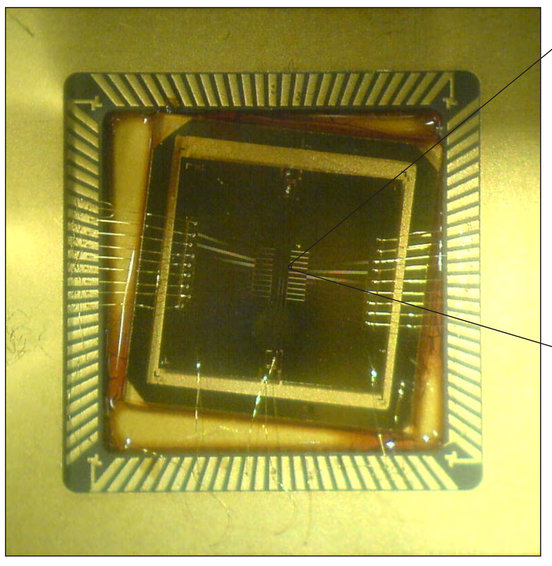
Lift-Off:
+ Simple process
+ High resolution (~2 µm)
+ Low surface roughness (~1 nm)
- Low electrode thickness (<1000 nm)

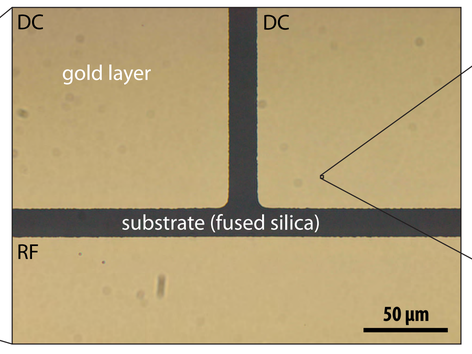
Electroplating:
+ High electrode thickness (>10 µm)
+ High resolution (~2 µm)
+ Low surface roughness (~2 nm)
- Complicated process

Electroplating Process

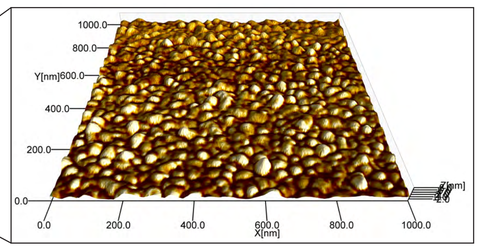


Our First Home-made Surface Ion Trap (Yedikule, Lift Off)





Light microscope picture



AFM picture of gold electrodes
(surface roughness R_q 1.16 nm)

- 9 segements (width: 175 µm)
- Ion-electrode distance: 130 µm
- Gap between electrodes 17 µm
- Gold electrodes (300 nm thick) on fused silica

Outlook

- **Fabricate and optimize new ion traps**
- **Measure heating rates of different traps at low temperatures (lift off, electroplating)**
- **Develop 2D arrays**
- **Implement entangling operations**