Two-dimensional ion trap lattice on a microchip

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Microfabricated ion traps are a major advancement towards scalable quantum computing with trapped ions. The development of more flexible ion trap designs, in which tailored arrays of ions are positioned in two dimensions above a microfabricated surface, would lead to applications in fields as varied as quantum simulation, metrology and atom-ion interactions. Current surface ion traps often have low trap depths and high heating rates, due to the size of the voltages that can be applied to them, limiting the fidelity of quantum gates. In this article we report on a fabrication process that allows for the application of very high voltages to microfabricated devices in general and we apply this advance to fabricate a 2D ion trap lattice on a microchip. Our scalable microfabricated architecture allows for reliable trapping of 2D ion lattices, long ion lifetimes due to the deep trapping potential, rudimentary shuttling between lattice sites and the ability to deterministically introduce defects into the ion lattice.

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The introduction of microfabrication techniques to the field of ion trapping has lead to the development of impressive microfabricated radio-frequency (rf) ion trap devices [1]. Using such devices, all the building blocks for scalable quantum computing have been demonstrated [2], including ion combination and separation and junction shuttling [3, 4] as well as two-qubit gate operations [5].

A drawback of current microfabricated ion traps stems from the ions at the rf nil naturally forming a 1-dimensional string, so far, limiting their usefulness for applications that require the formation of arbitrary 2-dimensional (2D) ion lattices. Penning traps offer a platform for a 2D lattice of ions, but the rotating crystal makes individual ion addressing and readout experimentally challenging, and the lattice geometry is limited to the naturally forming Wigner crystal [6].

The applications for a 2D ion lattice are numerous and far reaching, including, among others, spatial B-field and E-field sensing [7, 8], force detection [9], interactions between neutral atoms and ions [10] and cluster state quantum computing [11].

A further exciting application for a 2D ion lattice is in the field of analogue quantum simulation where the Hamiltonian of a complicated many-body system can be realised and its properties measured [12, 13]. A promising approach to realising a 2D quantum simulator constitutes the proposal to use a two-dimensional lattice of individual rf ion traps [14–16]. Each lattice site contains a single ion which interacts with neighbouring ions via the Coulomb force. The current challenge lies in developing microfabrication techniques that allow for a tightly spaced ion lattice to be obtained where the ion-ion separation is small enough for coherent interactions to be measured. To date, experimental progress towards such a lattice has been limited to trapping dust particles and ion clouds above PCB boards [17] or wire meshes [18]. The optimum trap geometry of such a device has been well studied [19, 20].

In operating a microfabricated ion surface trap, restrictions on the rf voltage that can be applied due to low flashover voltages exist [1, 21] and prohibit a large trap depth and ion-electrode distance, d. This limits the achievable ion lifetime and secular frequencies and results in large heating rates of the ion motion which scales as d^{-4} [22] where heating has adverse effects on the fidelity of motion dependant qubit gate operations [23]. The ability to apply large voltages to MEMS devices also has application in nanoelectrospray thruster arrays for spacecraft [24–27], where high electric fields are desirable and may also be useful in microfabricated mass-spectrometry [28] as well as particle and cell sorting [29].

Here, we report on a general microfabrication process to achieve large breakdown voltages in microfabricated devices and use this process to fabricate a 2D lattice of ion traps on a microchip. This process could also be used for other surface electrode ion trap geometries. Using this chip we demonstrate trapping of a 2D lattice of single Yb^{+} ions, the deterministic trapping of multiple ions at lattice sites and rudimentary ion shuttling between lattice sites. The device presented is suitable for 2D sensing applications. The ion-ion distance for this device is however too large to be used for quantum simulation. We discuss how a simple modification to the microchip design would allow for simulation of 2D spin lattices. This modified design would also offer possible architectures for 2D cluster state generation [11] and general quantum information processing [14]. Since the device presented in this article is

an integrated ion trap chip [1] it is scalable to much larger ion lattices.

I. RESULTS

Fabrication of the microchip. The layered structure of a commercial silicon-on-insulator (SOI) wafer was used by Britton *et al.* [30] to fabricate a linear ion trap permitting the application of voltages of up to 150 V. We have developed a different fabrication process using a SOI wafer to fabricate a planar ion trap with a significantly increased trap depth whilst maintaining large ion-electrode separations using a combination of recessed electrodes and the application of voltages in excess of 1 kV. We describe both of these fabrication advances in more detail below.

We utilise the layered SOI wafer to form a planar trap electrode structure, with a 2D electrode pattern but instead of the ground electrodes lying on the same plane as the rf electrodes they are recessed from the chip surface. This recess was achieved by using the SOI handle layer as rf ground, shown in Fig. 1C. By using recessed electrodes the trap depth for a given ion-electrode separation and voltage can be substantially increased.

To ensure ions can be trapped at a large ion height while maintaining a deep trapping potential using microfabricated ion traps in general and our lattice ion trap specifically a fabrication process that allows for high voltages to be applied was developed. This process not only has use for ion trap fabrication but for other microfabricated and microelectromechanical systems (MEMS) devices in general. We chose a thick oxide layer thus increasing the path length between the electrodes and the handle layer as well as reducing capacitance between the rf electrode and ground. However this would typically only result in a modest increase in breakdown voltage. We were able to obtain a much larger increase by using a specialised fabrication process. In order to explain this process it is important to note that voltage breakdown will usually occur via insulator surfaces connecting two conductors rather than through the insulator bulk. We selected a particular SOI structure that was fabricated by wafer bonding two wafers with 5 μm thick oxide surfaces to form a 10 μm thick buried oxide layer. Using a buffered HF etch, lasting $130 - 140$ minutes, the oxide layer was etched to expose the handle layer. As there is an increased etch rate on the interface where the two oxide layers were bonded together a highly anisotropic etch results laterally under the electrodes. Rather than obtaining the usual approximately straight etch profile, we were able to obtain the V-shaped undercut as shown in Figs. 1D and 2B. This V-shaped etch profile substantially increases the path length between the electrodes and ground resulting in extremely high breakdown voltages as it increases the effective distance for surface flashover from 10 μm to up to 120 μm. Electrical flashover measurements were performed on SOI test samples to determine the voltage that can be applied (see Methods). The mean flashover voltages were measured to be $V_{dc} = 1298(78)$ V and $V_{rf} = 1061(10)$ V, where the error is the standard deviation. These values are one or two orders of magnitude higher than in previously fabricated microfabricated ion traps [1, 30]. In fact these voltages correspond to typical values applied in traditional ion traps made using large metallic rods illustrating the impressive performance of our microchip.

The microchip consists of 29 traps arranged in a triangular lattice, with each ion having up to six nearest neighbours with an ion-ion separation of 270.5 μm. The ion-electrode separation is 156 μm. Due to the recessed ground electrodes the ion height from the top of the trap surface is 116 μm, as seen in Fig. 1D. A 3D contour plot of the trap potential for the central 11 trap sites is shown in Fig. 3B, a 2D contour plot is projected below showing the potential at the ion height. To adjust the position of the ions to compensate for stray electric fields and perform shuttling operations quasi-static voltages can be applied to six electrodes (Comp 1-6) which surround the rf electrode.

Trapping and manipulation of ions on the microchip. An rf voltage $V_0 = 455(3)$ V at a frequency $\Omega/2\pi = 32.2$ MHz was applied to the rf electrode to produce a trapping potential. All other electrodes were initially held at ground. A flux of neutral ytterbium atoms travelling parallel to the trap surface was produced by ohmically heating a natural abundance ytterbium oven from which ^{174}Yb atoms were resonantly ionised using a two-colour photoionisation process with light at 399 nm and 369 nm. Trapped ions were then Doppler cooled by the 369 nm light, with 935 nm light used to repump the ion from a long-lived D-state. The cooling and ionisation laser beams were highly elliptical, forming a light sheet co-propagating parallel to the trap surface. An image plane co-incident with the plane of trap centres above the microchip was imaged onto an electron multiplying CCD array to view the ions.

The ion secular frequencies along the trap principle axes were measured to be $(\omega_{x'}, \omega_{y'}, \omega_{z'})/2\pi = (1.58, 1.47, 3.30) \pm 0.01$ MHz respectively, for a single ion trapped in the top right corner of the array. Using these measurements, numerical simulations of the trap predict a trap depth of 0.42(2) eV. The lifetime of a single laser cooled ion was ~ 90 minutes,

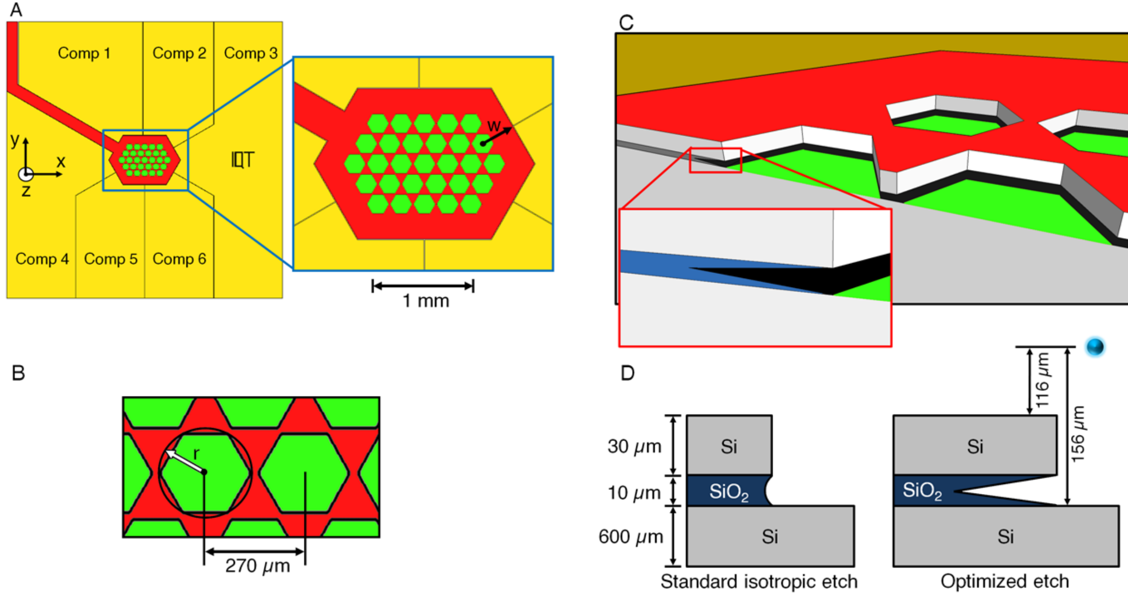

Figure 1: (**A**) The electrode design for the microchip. The rf electrode is shown in red, compensation electrodes are shown in gold and the ground electrode is shown in green. There are 29 trapping sites, one above the centre of each hexagon of ground electrode. The distance from the outer polygon centre to the rf edge, labeled w, is 410 μm. (**B**) Close-up of the hexagonal trap geometry with a polygon radius r = 125 μm and neighbouring traps separated by 270.5 μm. (**C**) Cross-section drawing of the trap geometry, showing the SOI layered geometry. The close-up inset shows the deep V undercut achievable with our fabrication process. (**D**) Two schematics of the etch profile, a typical isotropic etch is shown on the left, showing a slight undercut into the buried oxide. The right picture shows the profile of our optimised etch. The preferential etch rate along the bond face results in a deep V-shaped undercut. The ion height relative to the trap electrodes is also shown.

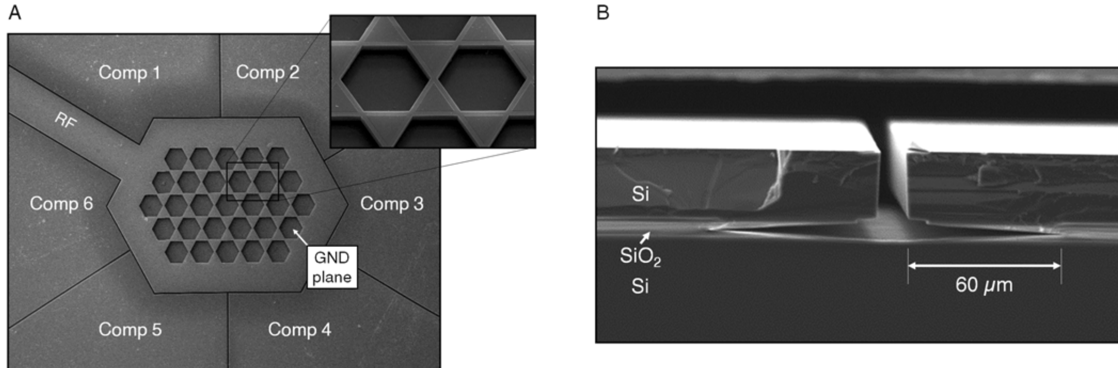

Figure 2: (**A**) An SEM of a finished microchip. The inset shows a close up of two of the hexagonal traps, this shows the recessed ground electrode. (**B**) An SEM cross section of the layered SOI structure at the interface between two compensation electrodes. The deep V-shaped undercut into the oxide layer is clearly visible extending 60 μm into the SiO_2 layer.

likely limited by background collisions and $\gtrsim 5$ minutes without cooling light.

A 2D ion lattice can be seen in Fig. 3A, six ions are trapped in adjacent lattice sites, with the viewable area limited by our imaging system. While producing such a uniform lattice is difficult when the 399 nm photoionisation laser uniformly illuminates the trap due to the stochastic nature of loading, by steering the ionisation beam to address specific sites of the lattice we can controllably fill the

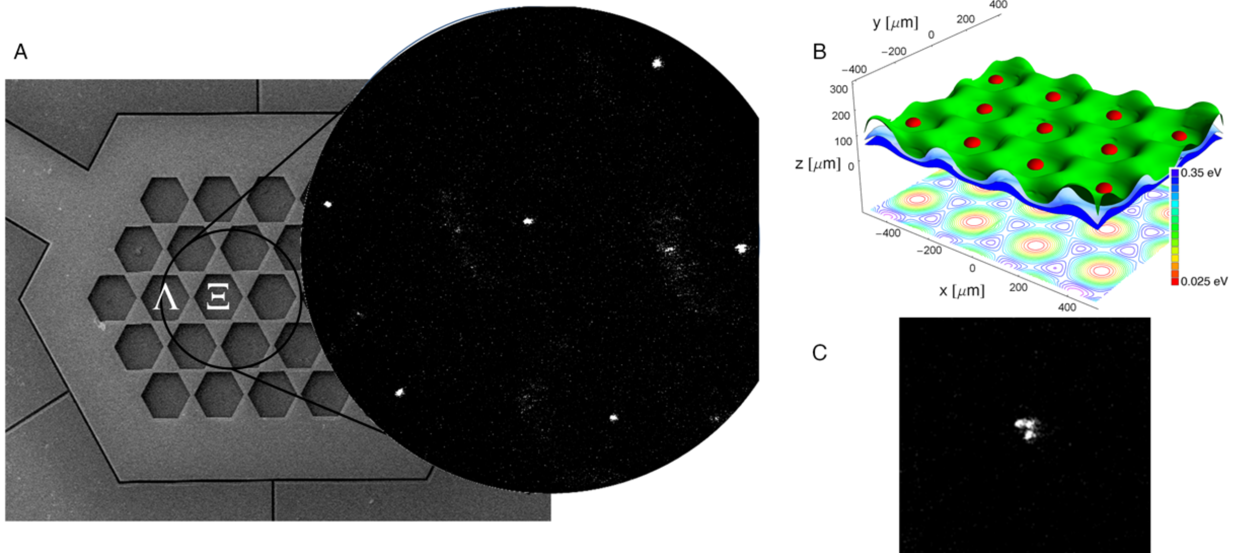

Figure 3: (**A**) A CCD image of six ions trapped simultaneously on the lattice is shown, the hexagonal shaped electrodes are also visible due to laser scatter. The area imaged was limited by our current imaging system and marked by a black circle over an SEM image of the trap. (**B**) A 3D contour plot of the lattice potential for the central 11 trap sites with an rf voltage of 455 V. The equipotential surfaces correspond to: red = 0.04 eV, green = 0.4 eV, light blue = 0.5 eV and blue = 0.6 eV. A 2D contour plot of the potential at the ion height is projected below, the equipotential lines are separated by 0.04 eV. (**C**) A CCD image of a single lattice site containing a three-ion Coulomb crystal.

lattice. We can also introduce defects, either empty sites or multiple ions per site, in the same manner. A three-ion defect is shown in Fig. 3C. Such lattice defects may be of interest when investigating Bose-Hubbard physics, such as superfluid-Mott insulator transitions or simulations of spin models with spin greater than 1/2.

We have also demonstrated shuttling of ions between different sites of the lattice. An ion is initially trapped at site Ξ, as marked in Fig. 3A. By lowering the rf voltage to minimise the potential barrier and applying control voltages to the surrounding electrodes, the ion is shuttled to position Λ. Figure 4 shows two CCD images of the ion before and after shuttling, also shown are the typical shuttling voltages. To shuttle the ion back to Ξ the polarity of the voltage on Comp 3 and Comp 6 is reversed. While this shuttling was performed using global control electrodes, enhancing the trap design by adding local control electrodes around each trapping site would allow the distribution of ions over the lattice sites to be changed after the ions are loaded. This would enable separate loading and experiment zones, and for the lattice to be repaired if an ion is lost due to a background collision. Such local control would also enable precise control of the micromotion at each site.

II. DISCUSSION

A 2D lattice such as we demonstrate here has many potential future applications. The use of single ions for highly sensitive magnetic-field sensing has been demonstrated [7], and the use of a lattice would allow for spatial as well as temporal measurements. Single ions have been proposed to be used as point imperfections inside Bose-Einstein condensates [10], and ion lattices would allow the effect of precisely tailored arrays of imperfections, both regular and irregular depending on microchip design, to be studied.

One important future application for a 2D ion lattice is in the field of quantum simulation, where trapped ions represent spins in solid-state systems, and the interactions between spins can be tailored to create analogues of different 2D systems (such as Ising or Heisenberg spin lattices) in a clean, controllable and easily interrogated manner.

In simulating these systems, interactions between ions trapped in adjacent sites a and b would be mediated by the Coulomb interaction. The coupling between motional states $H_{\mathrm{Coul}} = -\hbar\Omega_{\mathrm{ex}}/2(a^{\dagger}b + ab^{\dagger})$ where $a, a^{\dagger}, b, b^{\dagger}$ are the phonon annihilation and creation operators for the two sites, and the coupling

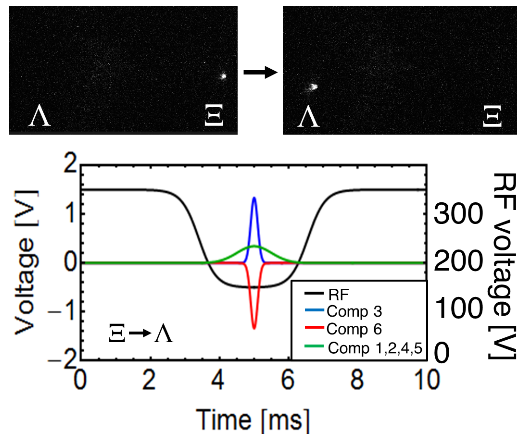

Figure 4: Two CCD images are shown before and after shuttling an ion from lattice site Ξ to Λ. The shuttling voltage profile for this shuttling operation is shown. To shuttle the ion back to Λ the polarity of the voltages on Comp 3 and 6 is reversed.

strength

$$\Omega_{\rm ex} = \frac{e^2}{2\pi\varepsilon_0 m\omega}\frac{1}{r^3} \tag{1}$$

for a pair of singly-charged ions of mass m confined in traps with secular frequency ω separated by distance r [31, 32].

For the lattice we have presented here, where $r = 270.5\,\mu$m and with a trap frequency of 1 MHz, the coupling strength $\Omega_{\rm ex}/2\pi$ would be only 2 Hz, impractical for performing simulations and very small compared to the strengths already experimentally demonstrated using linear surface traps [31, 32]. The coupling strength has a very strong dependence on the ion-ion separation ($\Omega_{ex} \propto r^{-3}$) and reducing this distance would be key to obtaining useful couplings. A lattice based on smaller ion-ion distances can easily be designed and produced using the fabrication method presented in this paper.

Using an SOI wafer with a 2.5 μm device layer and a 2.5 μm oxide layer fabricated by wafer bonding two 1.25 μm oxide layers together would reduce the depth of the ground plane beneath the surface of the microchip to 5μm, and a trap electrode design with a hexagon radius of 13 μm and hexagon centre separation of 32 μm fabricated on such a wafer would produce a lattice of traps 15μm above the surface of the microchip. For a trap frequency $\omega/2\pi$ of 1 MHz, the motional coupling strength $\Omega_{\rm ex}/2\pi$ would then be 1.3 kHz, a thousandfold increase compared to our current chip design. This value is comparable to previously achieved coupling strengths between individual wells in linear traps [31, 32].

If this trap were used to simulate a 2D spin lattice using the scheme proposed by Porras and Cirac [15, 33] a spin-spin coupling strength $J \approx 2\pi \times 1$ kHz would be obtainable using a 355 nm laser of 900 mW power (see methods). It is also important to consider possible sources of decoherence to evaluate if a successful quantum simulation is expected for this prospective trap. We consider both heating of the motion of the trapped ions and photon scattering due to the laser driving the gate. These rates should be low compared with the spin-spin coupling strength J. At such small ion-electrode distance, heating rates at room temperature will be many orders of magnitude greater than J, necessitating cooling of the chip. While estimating heating rates is imprecise, a best estimate (see methods) for a trap of this design operating cryogenically at 6 K is $\dot{n} \sim 540\,s^{-1}$ based on previous experiments [34]. The photon scattering due to the coupling laser is estimated to be $10\,s^{-1}$. Both these rates are much less than J indicating that this type of quantum simulation should be possible with this combination of chip and driving laser.

We have demonstrated a 2D ion lattice integrated on a microchip along with a fabrication process to significantly increase the voltage that can be applied to microfabricated devices. By increasing the breakdown voltage, both 2D lattice and linear surface traps with higher trap depth and lower heating rates (by making use of larger ion-electrode distances) can be fabricated. For surface traps built to perform quantum information processing this reduces the effects of motional heating on gate fidelities [23]. Additionally, we have used this advance to demonstrate the operation of a 2D lattice of ytterbium ions on a chip which offers many potential uses including 2D force measurement, B-field and E-field sensing and with modifications may offer a platform for quantum simulations.

III. METHODS

Surface flashover measurements. Surface flashover measurements were performed on test chips consisting of gold coated silicon islands surrounded by the exposed handle layer. The chips were glued, using conductive silver glue, onto a ceramic chip carrier and placed in high vacuum at a pressure of 6×10^{-4} Pa. Radio-frequency voltage was applied by connecting a quarter-wave helical coil resonator to the vacuum feedthrough. This ensured > 90 % coupling between the rf amplifier and chip at a resonant frequency of 28.0 ± 0.5 MHz with $Q = 210 \pm 15$. The rf voltage was steadily increased while observing the sample. Upon breakdown the voltage was measured using a capacitively coupled probe.

Radio-frequency flashover was observed to occur ≈ 20 % lower than static flashover. The exact cause for this is not known, however it is likely a result of local heating on the chip and outgassing from the surface when the rf voltage is applied. To apply sufficient voltage to trigger flashover, up to 30 W of rf power was applied to the chip. This power would be predominately dissipated on chip, which has the largest impedance. This would result in significant heating of the chip and the release of gases previously adsorbed to the surface.

Mounting of microchip inside the vacuum system and application of voltages. The trap was mounted onto a ceramic chip carrier, with gold ribbon wire connecting the electrodes to the chip carrier bond pads. The chip was mounted inside a UHV vacuum system at a pressure of 8.0×10^{-8} Pa. To ensure good rf grounding 820 pF capacitors were wire bonded to the static electrodes. The radio frequency voltage was applied via an external helical coil resonator with $Q = 160$ to provide voltage amplification and filtering of unwanted frequencies [35].

Calculation of quantum simulation parameters for modified microchip design. The Porras and Cirac spin simulation scheme [15, 33] requires a state dependant force to be applied to the ions whose internal states encode the simulated spins. The effective spin-spin coupling rate is given by $J = \beta F^2/4\hbar m_i \omega_i^2$ where $\hbar = h/2\pi$, h is Planck's constant, $\beta = \Omega_{ex}/\omega_i$ and F is the magnitude of the state dependant force applied to each ion [15]. For the proposed modified chip design, with its ion-ion separation of 32 μm and using a laser with a wavelength of 355 nm and a power of 900 mW focused into a light sheet of width 160 μm and depth 30 μm, a coupling strength $J \approx 2\pi \times 1$ kHz could be achieved. Since the simulation is driven by the displacement of the ions due to the force F, the simulated spins are entangled with the motional state of the ions at the end of the simulation. This produces an error in the measured spin properties of the simulated system proportional to F^2 [33]. For the proposed modified design we calculate a simulation error due to this effect of ≈ 25 % for the measurement of single-particle properties of the simulated system. In addition to using lasers to produce the spin-spin coupling, magnetic field gradients could also be used to generate the required spin-dependent forces [36] and would allow individual addressing of ions.

Motional heating on an ion is a result of the electric-field noise density at the ion at the trap secular frequency ω, $S_E(\omega)$. For the proposed modified chip we assume that the electric-field noise density is consistant with previous experiments at a temperature of 6 K [34] and estimate $S_E(\omega) \approx 1.6 \times 10^{-11}$ $\mathrm{V^2m^{-2}Hz^{-1}}$ (see Fig. 20 in Ref.[1]). This results in a heating rate $\dot{n} = 540\, s^{-1}$.

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V. AUTHOR CONTRIBUTIONS

R.C.S. planned the experiment, designed the microchip and the fabrication process, performed the experiment and wrote the manuscript, H.R. fabricated the microchip, S.W., K.L. and S.C.W. performed the experiment and assisted in writing the manuscript, P.S. and M.K. assisted in the development of the fabrication process and W.K.H. planned the experiment, coordinated the work, helped design the microchip and fabrication process and assisted in writing the manuscript.

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